13.1 A 9.95 to 11.1Gb/s XFP Transceiver in 0.13μm CMOS

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The XFP module is a small-footprint serial-IO protocol-agnostic multi-rate optical transceiver, intended for telecom (SONET OC-192) and datacom (10Gb/s Ethernet and 10Gb/s fiber channel) applications [1]. Figure 13.1.1 shows a typical XFP module. The optical receiver (RX), retimes the output of a transimpedance amplifier and delivers a serial 10Gb/s signal to the host. The transmitter (TX) retimes a serial data stream that has potentially crossed 9.25 inches of FR4 PCB. A monolithic signal conditioner that provides these retiming functions, as shown in Fig. 13.1.1, is described.

Figure 13.1.2 shows the transceiver architecture. The RX path consists of a limiting amplifier with a sensitivity of $10mV_{ppd}$,a CDR, and an output driver. The TX path is identical to the RX path with the exception that it includes a linear equalizer to compensate for dispersion jitter from 9.25 inches of FR4 PCB.

The CDR has a frequency-acquisition loop, a delay- and phase-locked loop, and a drift-compensation loop. At startup, the frequency-acquisition loop that includes a frequency detector, a charge pump, and the VCO, adjusts the output frequency until its divided value is within 500PPM of the 155.5MHz reference clock for 9.95Gb/s.

The data signal path employs a dual-loop architecture with a DLL and a PLL [2]. An advantage of the dual-loop architecture is that it allows separate jitter-tolerance and jitter-transfer bandwidths, each optimized for manufacturing robustness. Furthermore, there can be less jitter at the output of the signal conditioner relative to its input easing the jitter tolerance requirements of subsequent CDRs in the host system.

The jitter-tolerance bandwidth for a dual-loop CDR is determined by the DLL path. It includes the phase detector, the charge pump and the data phase shifter [2]. Previously reported dual-loop CDRs use a linear phase detector for which a 3dB-tolerance bandwidth can be calculated. This CDR employs a binary phase detector in the DLL. A frequency response for the DLL cannot be defined, because the binary phase detector has a nonlinear transfer function [3]. Instead, jitter tolerance is set by the slew rate of the DLL, which is $2DF*I_{cp}*psh/Cp$ (rads/s) where DF is the transition density, I_{cp} is the charge-pump current, psh is the phase-shifter gain, and Cp is the charge-pump capacitor.

Two paths from the output of the charge pump lead to the input of the phase detector. The first path through the phase shifter has a gain of psh, and the second path through the VCO has a gain of K_{vco}/s. The zero formed by subtracting these 2 paths is at a frequency K_{vco}/psh, where the PLL surrenders control of the retiming function to the DLL. As previously shown in [2], the jitter-transfer bandwidth of the dual-loop PLL occurs at the frequency of this zero, for sufficiently large phase-detector gain. Thus, the jitter-transfer bandwidth for this dual-loop CDR does not change with the amplitude of the applied jitter even though a binary phase detector is used.

The half-rate binary phase detector shown in Fig. 13.1.3 consumes less power and exhibits better performance than a full-rate binary phase detector. This half-rate phase detector differs from prior art [4] in that it has a 2:1 serializer. Quadrature clocks (CK0 and CK90) that are generated by dividing a full-rate clock, sample the center and the edge of the data eye. The 2:1 serializer takes data from clock domain CK0 and outputs full-rate serial data on clock domain CK90. It is important to serialize the data on CK90 rather than CK0, as it is CK90 that is phase aligned to the incoming data edges.

Clock drivers in the phase detector are implemented as programmable LC tanks. An FSM within the clock drivers tunes the tank resonance by switching MIM capacitors so that the lowest power consumption is achieved. The LC tank has 4 advantages: consumes one-third of the power consumed by the equivalent RC-based clock driver, removes dc offsets, filters duty cycle distortion, and removes high-frequency jitter beyond the bandwidth of the tank which is typically 500MHz.

To cover the frequency span from 9.95 to 11.1Gb/s over process and temperature variations, the VCO shown in Fig. 13.1.4 has 3 cores; each with 5b binary-weighted switched MIM capacitors. Within each core, a coarse tune varactor is driven first by the frequency charge pump to tune out LSB error and second, by the drift-compensation loop which tracks center-frequency variations with temperature and leakage currents on the CF capacitor. This separation of rate, process, and temperature tracking minimizes coarse tune varactor gain providing low phase noise, -112dBc/Hz @1MHz measured, and low jitter generation. Tank swings are AGC controlled to linearize thick-oxide triple-well inversion-mode NMOS varactors with their backgate tied to source/drain, achieving 1.3 to 1 K_{vco} variation, which provides good control of the transfer bandwidth. The VCOs also employ triple-well NMOS devices with their backgate referred to supply to achieve 1MHz/V or 20ppm supply pushing.

A linear equalizer in the transmit path compensates for dispersion from up to 9.25 inches of FR4 PCB. Without equalization, the resulting eye closure would prohibit the loop from locking. Moreover, NRZ data applied to a channel with a low-pass characteristic has bimodal jitter in the resulting data eye. This bimodal jitter creates a deadband in the transfer function of the binary phase detector that leads to excessive jitter generation. For these reasons, a first-order passive equalizer precedes the limiting amplifier on the TX side.

Figure 13.1.5 shows jitter generation from the TX path after 9.25 inches of FR4 PCB both before and after the signal conditioner. Jitter measurements are made using an Agilent 86100C DCA-J oscilloscope. Random jitter, RJ_{rms}, at the TX output is 3.59mUI which beats the XFP specification of 7mUI for random jitter.

Figure 13.1.5 also shows jitter-tolerance and jitter-transfer measurements. Jitter tolerance exceeds the SONET specification by a factor of 3 at all frequencies. The jitter transfer bandwidth is 3.6MHz, and changes hardly at all for different amplitudes of applied jitter.

Acknowledgments:
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References:
[1] "10 Gigabit Small Form Factor Pluggable Module (XFP) MSA", rev. 4.0, Apr. 13, 2004.
[2] T. Lee, and J. Bulzacchelli, "A 155-MHz Clock Recovery Delay- and Phase-Locked Loop," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1736-1746, Dec., 1992.
[3] R.C. Walker et al., "A Two-Chip 1.5-GBd Serial Link Interface," *IEEE J. Solid-State Circuits*, vol. 27, pp. 1805-1811, Dec., 1992.
[4] J. Hauenschild, et al., "A Plastic Packaged 10GBPS Clock and Data Recovery 1:4 Demultiplexer with External VCO," *IEEE J. Solid-State Circuits*, vol. 31, pp. 2056-2059, Dec., 1996.

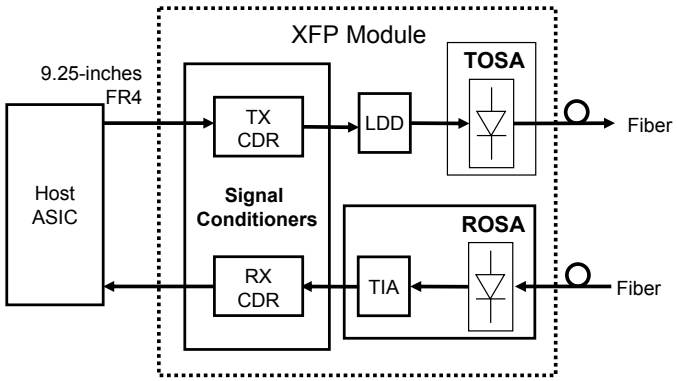


Figure 13.1.1: XFP Module.

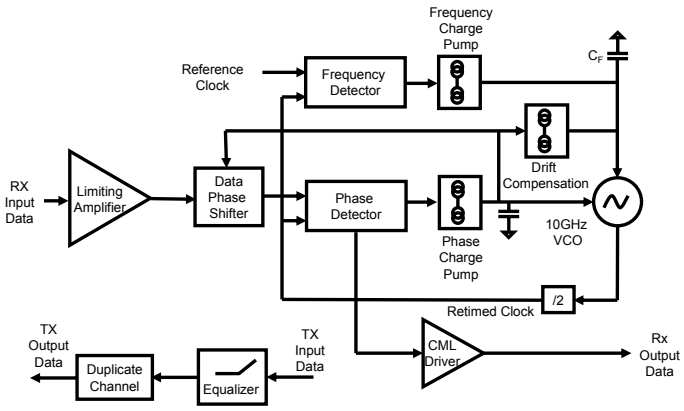


Figure 13.1.2: Transceiver architecture.

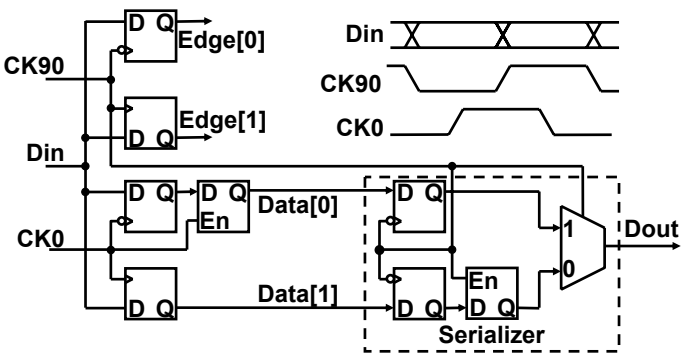


Figure 13.1.3: Half-rate binary phase detector with serializer.

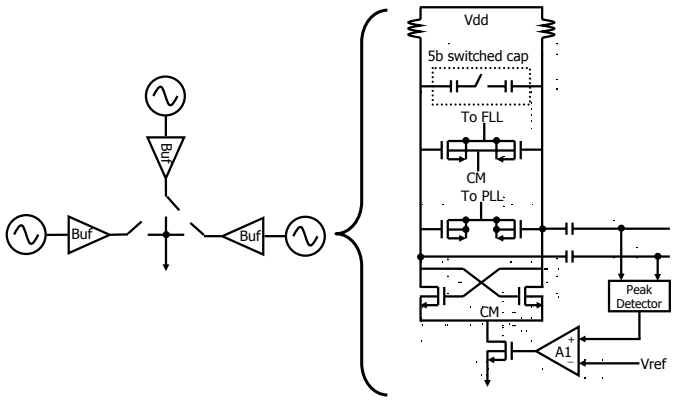
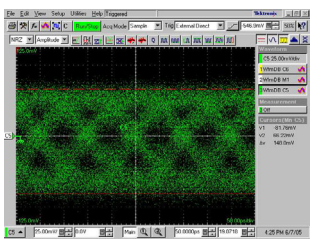
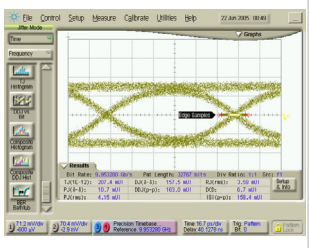
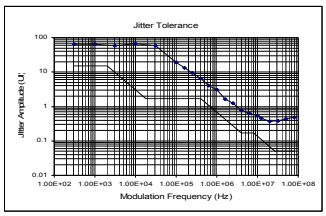


Figure 13.1.4: Voltage-controlled oscillator.







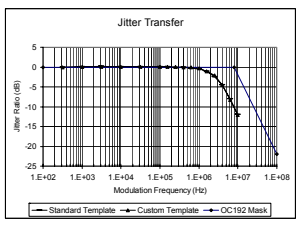


Figure 13.1.5: Jitter after 9.25-inches FR4, jitter generation, jitter tolerance, and jitter transfer.

Process Technology	8M 0.13µm
Die Area	4mmX2mm=8mm^2
Package	6X6 BGA
Input Sensitivity (PRBS7)	10mV
Jitter-Transfer Bandwidth	3.6MHz
rms Jitter (PRBS31)	3.59mUI
Total Power Consumption 1.8V Supply 3.3V Supply	793mW 385mA 30mA

Figure 13.1.6: Performance summary.

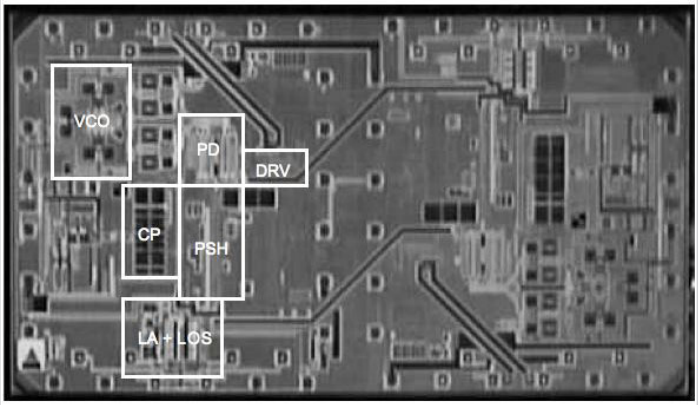
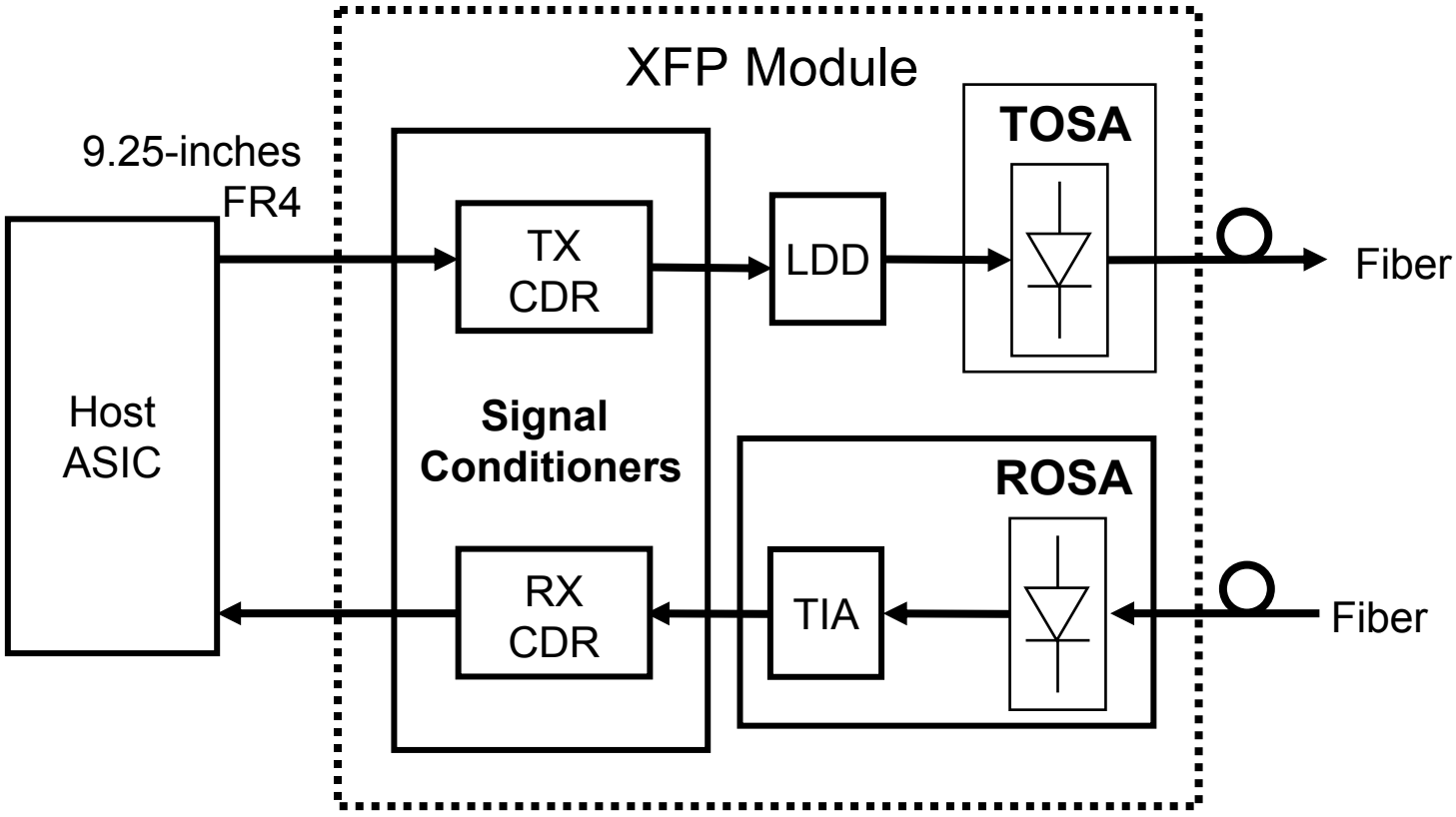


Figure 13.1.7: Die micrograph.



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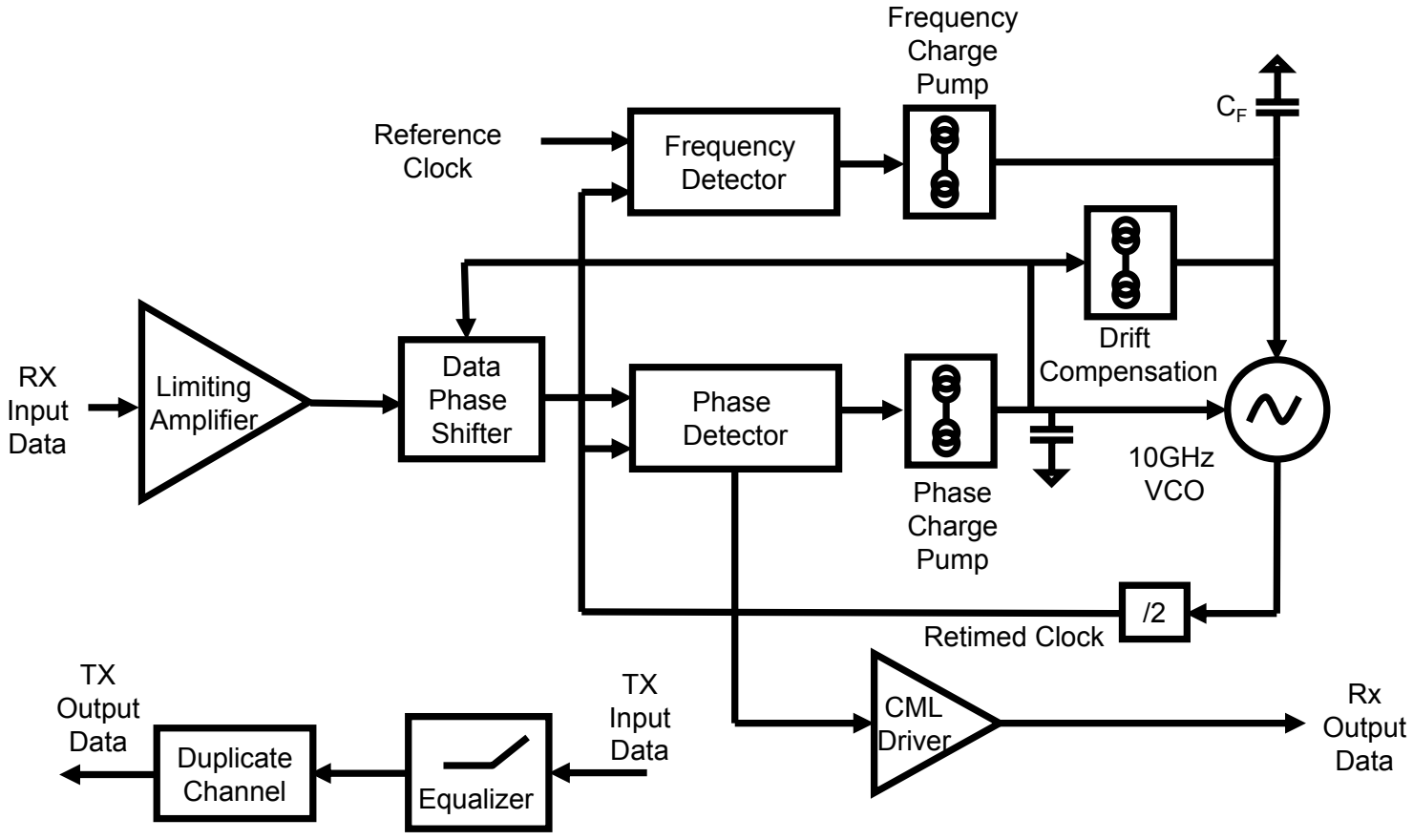

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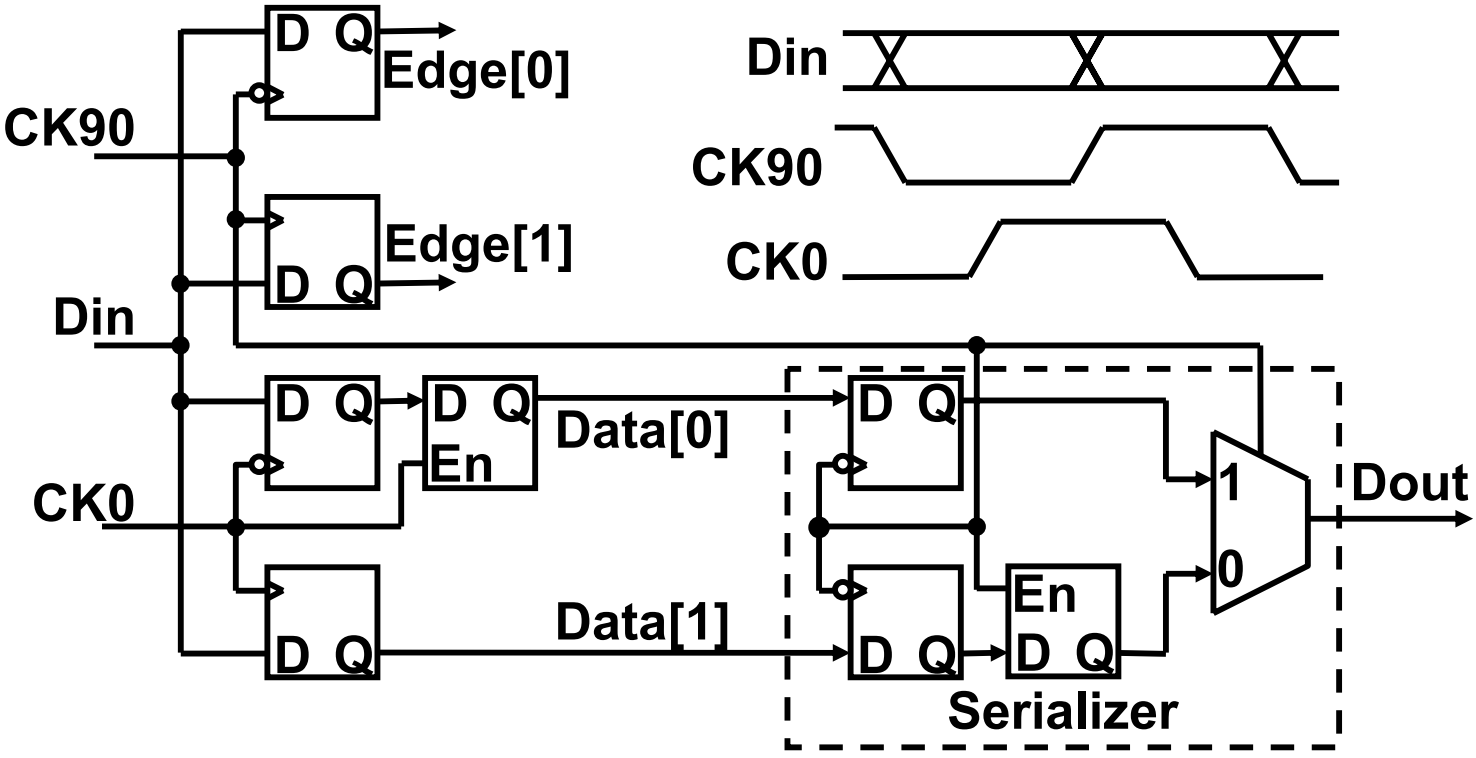

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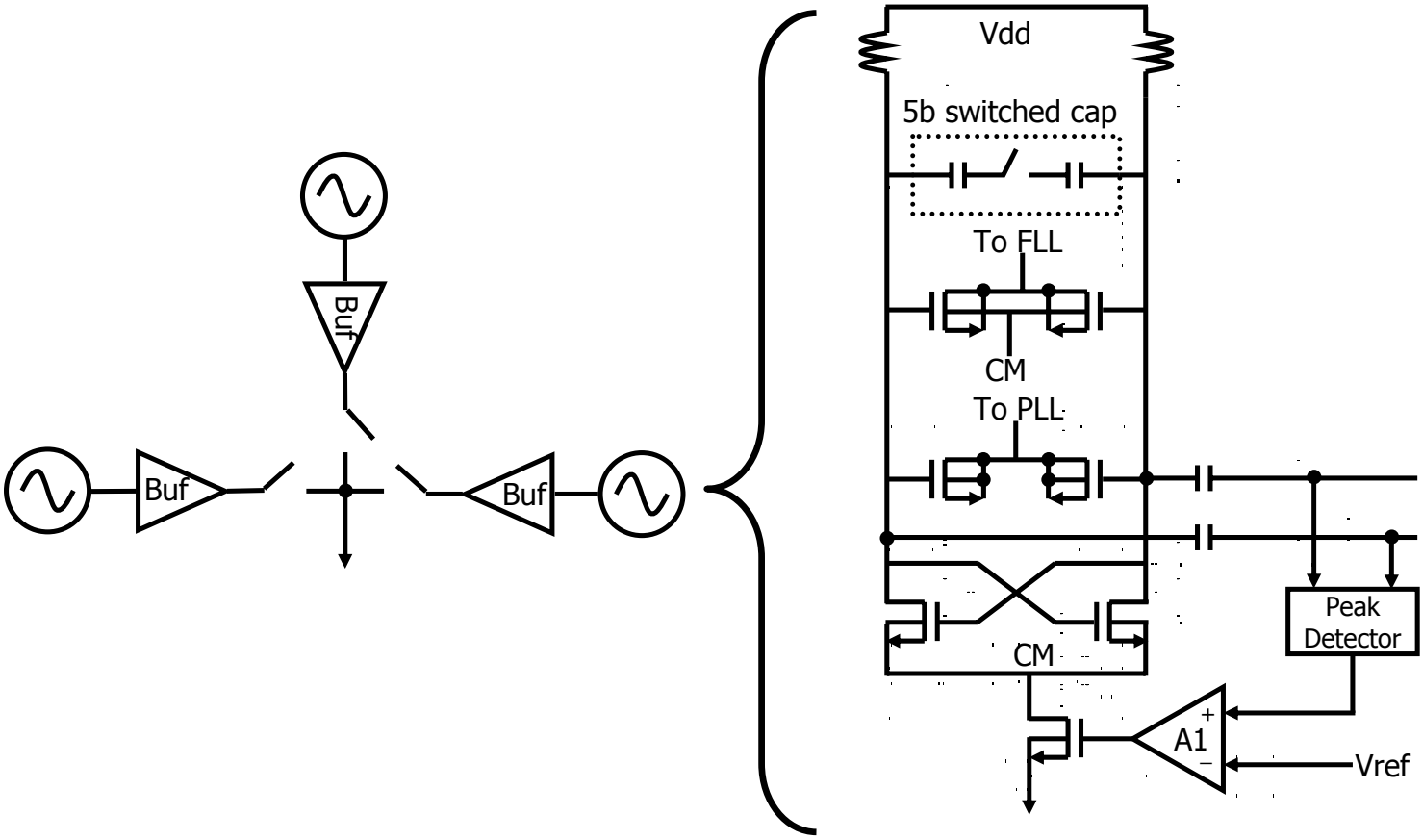

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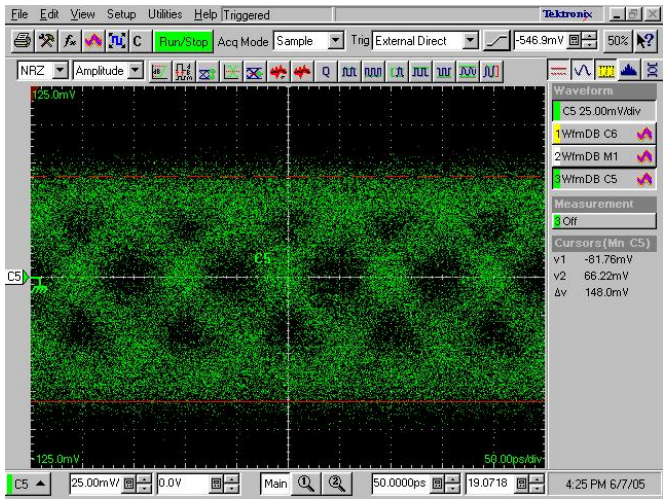

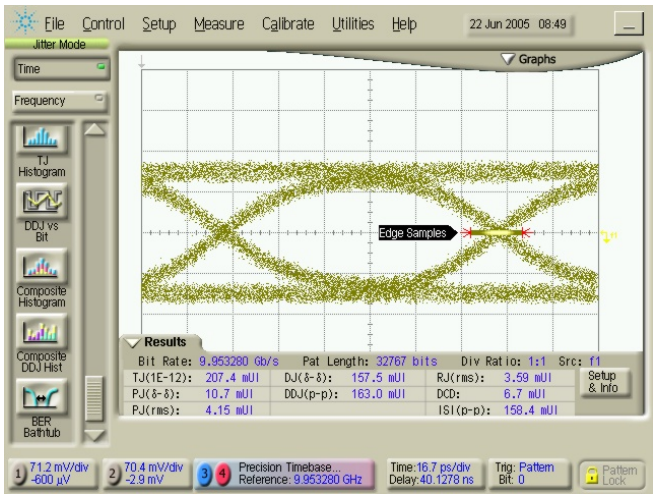

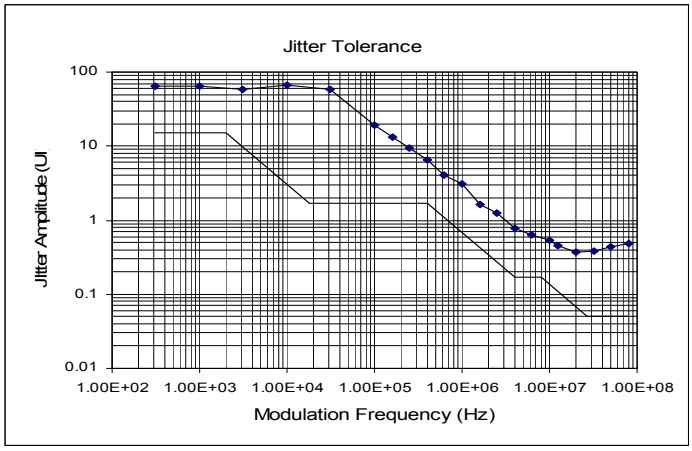

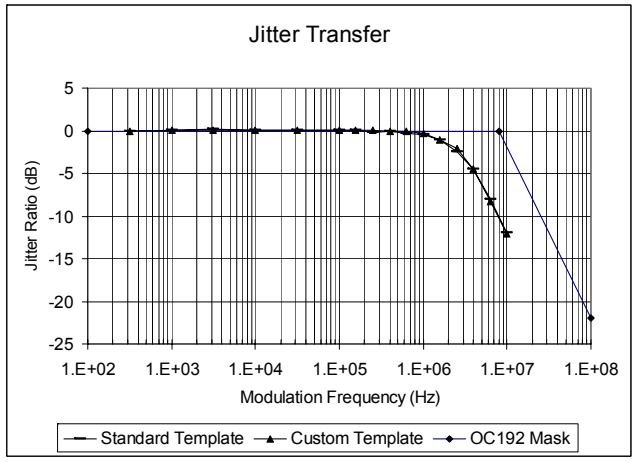

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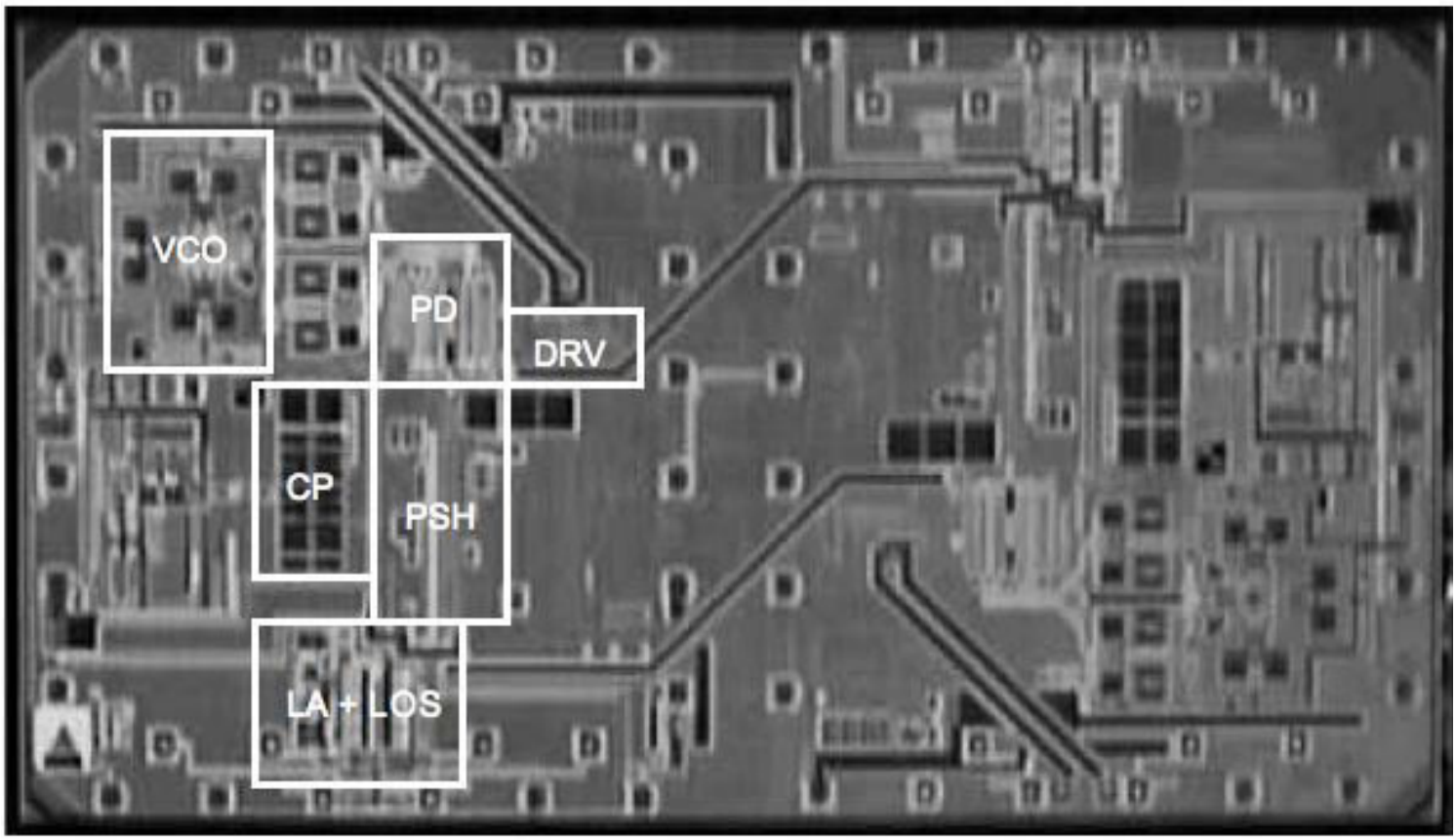

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