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''Square Root Domain'' Filter Design and Performance

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Abstract. This paper discusses the implementation and performance of square root domain filters, which can be considered as the CMOS equivalent of the bipolar log domain technique. The square root design methodology is based on exploiting the MOSFET large-signal square law characteristic to implement filters which are input-output linear, but operate with internally non-linear signals. The design of subcircuits required for the implementation of square root domain filters is described based on the MOSFET translinear principle, and various performance issues are discussed. Simulation and measured results are also presented to confirm the validity of this approach, which may be attractive for low-voltage operation at frequencies in the MHz range.

Key Words: analog integrated circuits, analog filters, CMOS translinear circuits

1. Introduction

The integration of analog and digital circuits on a silicon chip is constrained by the fact that most of the area is occupied by the digital circuitry, and consequently the fabrication technology is optimized for digital processing. Since digital circuits are fabricated almost exclusively in CMOS VLSI, the development of analog interface circuit design methodologies which are compatible with this technology is a topic currently attracting a great deal of interest.

Continuous-time filters are an important part of the interface circuitry between analog and digital parts of a system, for anti-aliasing filters for A/D and D/A converters, etc. The design of fully-integrated continuous-time filters presents various design constraints; a lack of high-Q integrated inductors necessitates the use of active elements, and variations in absolute component values (tolerances typically between 10–50%) means that the filter design parameters must generally be tuneable.

A class of integrated continuous-time active filters in CMOS technology known as ''MOSFET-C'' filters was first reported in 1983 by Banu and Tsividis [1]. These filters were derived from classical RC-active filters, where a MOSFET in the linear region of operation is employed as a tuneable linear resistance. The inherent non-linearities of the MOSFET resistors are cancelled by symmetrical circuit design [2]. Tuneability is limited by the fact that the MOSFET resistors should operate in the linear region, while the operating frequency range is limited by the need for opamps. Another important class of integrated continuous-time active filters are transconductor-C (gm-C) filters. These filters can inherently operate at high frequencies due to their open-loop topology [3]. However, there generally is a trade-off between speed, linearity and power consumption, and many different transconductor designs have been reported with emphasis on one or more characteristics such as linearity, high operating frequency, supply voltage, slew rate and tuneability [4,5].

Recently a new class of integrated continuous time filters have emerged in bipolar technology, known as ''log-domain'' or ''dynamic translinear'' filters. These circuits exploit the inherently non-linear exponential characteristic of bipolar transistors to implement circuits which are input-output linear, although internal signals are highly non-linear. Frey initially proposed a state-space design approach [6], whereby a

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set of linear state equations are transformed to a nonlinear (exponential) form. The resulting non-linear state equations are then directly implemented as the summation of bipolar transistor currents at internal nodes. Perry and Roberts introduced a technique enabling the signal flow-graph synthesis of log-domain LC ladder filters [7], and a method of log-domain filter synthesis based on the transformation of conventional gm-C filter architectures has also been described [8]. Following an alternative transistor-level approach, the low-level synthesis of log-domain filters has also recently been proposed [9]. For each of these methods, the resulting circuits generally exhibit the following features:

- Large-signal device equations are used in the circuit synthesis, therefore circuit operation is not limited to small-signal levels.
- The circuits are current-mode which offers potentially high speed properties (due to low impedance levels) and lower supply voltages [10].
- The circuits are easily tuneable through the variation of bias currents.

Micropower log domain circuits have also been implemented based on the exponential relationship between gate-source voltage and drain current in a subthreshold MOSFET. However, the operating frequency of subthreshold circuits is generally limited to the kHz range, which restricts their operation to very specific applications, e.g. biomedical sensors [11].

The attractive features of log-domain circuits, combined with the desire to implement analogue filters in CMOS VLSI technology, has led to the proposal of ''square-root domain synthesis'' as a new CMOS filter design methodology [12,13]. The proposed methodology uses MOSFET devices in the strong inversion region of operation, and thus is based on the quadratic relationship between gate-to-source voltage and drain current. This paper outlines the general concept and discusses various square root domain synthesis and performance issues. The paper is organized as follows: in Section 2, MOSFET square law synthesis techniques are reviewed and the generalized translinear principle is introduced; in Section 3, the state-space synthesis of square root domain filters is described; Section 4 discusses implementation issues and the validity of the square law approximation; Section 5 presents measured results and conclusions are given in Section 6.

2. CMOS Square Law Synthesis

The idea of exploiting the MOSFET square law characteristic to implement a required transfer function is not new, but until recently only real-time static circuit functions had been reported. A simple example is the linear transconductor shown in Fig. 1, proposed by Bult and Wallingra [14]. Assuming that the devices are in saturation, the square law relationship between drain current I_d and gate-source voltage V_{gs} is assumed as:

$$I_d = \beta(V_{gs} - V_{th})^2 \tag{1}$$

V_{th} and β represent the threshold voltage and transconductance parameter respectively. If the devices are matched (equal β and V_{th}), the resulting output current:

$$I_1 - I_2 = \beta(V_2 - 2V_{th})(V_2 - 2V_{\text{in}}) \tag{2}$$

thus for constant V_2, the output current is a linear function of V_{in}.

More complex linear transconductor designs have been reported based on the exploitation of the square law, which offer wider dynamic range, differential operation etc. [15,16]. Non linear circuit functions such as squarers and multipliers have also been proposed based on this methodology, e.g. [14,15,17–19].

Following a slightly different approach, Seevinck and Wiegerink proposed a CMOS square law version

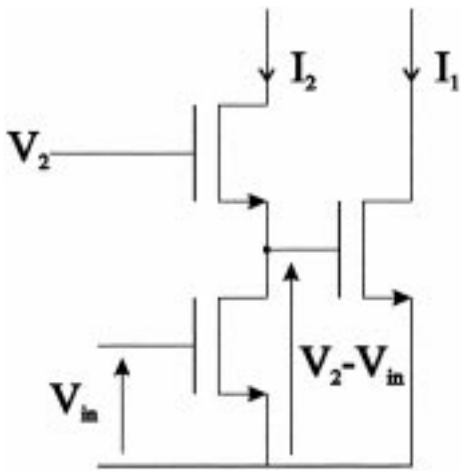


Fig. 1. Linear transconductor based on the MOSFET square law characteristic.

of the well-known bipolar translinear (BTL) principle [20], which they termed the MOS translinear (MTL) principle [21]. The MTL principle is a generalized synthesis methodology for the implementation of linear and non-linear circuit functions. An MTL loop contains an equal number of MOSFET gate-to-source voltages arranged clockwise (CW) and counterclockwise (CCW), thus the loop contains an even number of devices. If the loop contains both NMOS and PMOS devices, there must be an equal number of CW and CCW NMOS devices and an equal number of CW and CCW PMOS devices. An example of a NMOS MTL loop is shown in Fig. 2; summing the voltages around this loop and substituting the square law characteristic given in (1) gives the result:

$$\sqrt{\frac{I_{\mathrm{d1}}}{\beta_1}} + \sqrt{\frac{I_{\mathrm{d3}}}{\beta_3}} = \sqrt{\frac{I_{\mathrm{d2}}}{\beta_2}} + \sqrt{\frac{I_{\mathrm{d4}}}{\beta_4}} \tag{3}$$

For a general MTL loop containing N NMOS devices in each direction and P PMOS devices in each direction (thus total number of devices $= 2(N + P)$), the MTL principle is derived as:

$$\sum_{j,k=1}^{j=N,k=P} \left(\sqrt{\frac{I_{\mathrm{d}j}}{\beta_j}} + \sqrt{\frac{I_{\mathrm{d}k}}{\beta_k}} \right)_{CW} = \sum_{j,k=1}^{j=N,k=P} \left(\sqrt{\frac{I_{\mathrm{d}j}}{\beta_j}} + \sqrt{\frac{I_{\mathrm{d}k}}{\beta_k}} \right)_{CCW} \tag{4}$$

where I_{dj}, β_j represent the drain current and transconductance parameter of the jth N-channel device respectively, while I_{dk}, β_k relate to the kth P-channel device. Thus, the MTL principle can be stated as:

> The sum of the square roots of the drain currents divided by the transconductance parameters in the CW direction is equal to the sum of the square roots of the drain currents divided by the transconductance parameters in the CCW direction.

Although this expression is not as elegant as the BTL principle, the MTL principle can still be exploited to implement various non-linear circuit functions which will prove useful in the implementation of square root domain filters. An interesting feature of both BTL and MTL circuits is that input signals are applied as currents, and voltage swings within the circuit are of secondary interest. These ''internal'' voltage swings are additionally fairly small (changes in V_{be} or V_{gs}), leading to the potential for high frequency operation at low power supply voltages.

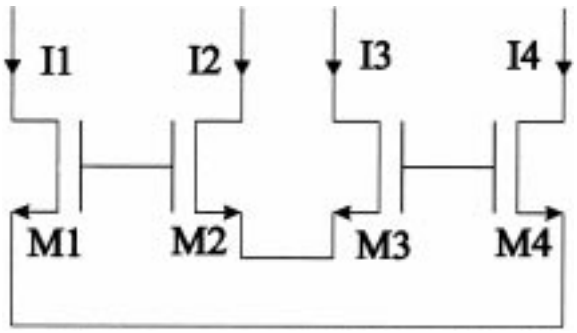


Fig. 2. A four-transistor NMOS translinear loop.

3. Square Root Domain Filter Synthesis

The concept of square-root domain filter synthesis has emerged as the square law equivalent of the exponential log-domain methodology. The general principle of square-root domain synthesis was discussed in [12], but Mulder et al. were the first to report a true square-root domain filter implementation in [13].

The design of a simple square-root domain circuit will be illustrated here by following a state-space mapping process, similar to the original log-domain methodology proposed by Frey [6]. Low-level integrator-based filter synthesis or LC-ladder synthesis methods proposed for log-domain filters can similarly be adapted for square root domain filters [24], and will not be discussed here. The aim of this paper is to present the general principle, and to discuss various issues which currently limit the performance of square root domain circuit implementations.

A second order filter can be described by the state equations:

$$\begin{aligned} \dot{x}_1 &= -\frac{\omega_o}{Q} x_1 - \omega_o x_2 + \omega_o u_1 \\ \dot{x}_2 &= \omega_o x_1 - \omega_o u_2 \\ y &= x_1 \end{aligned} \tag{5}$$

where u_1 and u_2 are input signals, y is the output, x_1 and x_2 are state variables, and a dot denotes time differentiation. ω_o and Q represent the natural frequency and quality factor of the filter. In a typical implementation one of the inputs is held constant,

while the other is used as the signal input. For example, if u_2 is held constant and the input is applied at u_1, the resulting bandpass transfer function can be derived:

$$H_1(s) = \frac{Y(s)}{U_1(s)} = \frac{\omega_o s}{s^2 + (\omega_o/Q)s + {\omega_o}^2} \quad (6)$$

Alternatively if u_1 is held constant and the input signal is applied to u_2, a lowpass transfer function can be derived:

$$H_2(s) = \frac{Y(s)}{U_2(s)} = \frac{\omega_o^2}{s^2 + (\omega_o/Q)s + \omega_o^2} \quad (7)$$

Consider a quadratic mapping on the state variables, such that:

$$x_1 = I_1 = \beta_1(V_1 - V_{th})^2$$
$$x_2 = I_2 = \beta_2(V_2 - V_{th})^2 \quad (8)$$

Substituting these variables into the linear state equations (5), and multiplying by constants C_1 and C_2:

$$\left(2C_1\sqrt{\beta_1 I_1}\right)\dot{V}_1 = -\frac{C_1\omega_o}{Q}I_1 - C_1\omega_o I_2 + C_1\omega_o I_{\text{in1}}$$
$$\left(2C_2\sqrt{\beta_2 I_2}\right)\dot{V}_2 = C_2\omega_o I_1 - C_2\omega_o I_{\text{in2}} \quad (9)$$

where the input signals u_1 and u_2 are replaced by currents I_{in1} and I_{in2} respectively, since the state variables have been transformed to current variables. Assuming that $C_1 = C_2 = C$ and $\beta_1 = \beta_2 = \beta$ for simplicity, and defining tuning currents $I_o = (\omega_o C)^2/\beta$ and $I_{oq} = I_o/Q^2$:

$$C\dot{V}_1 = -\frac{1}{2}\sqrt{I_1 I_{oq}} - \frac{1}{2}\sqrt{I_o\frac{{I_2}^2}{I_1}} + \frac{1}{2}\sqrt{I_o\frac{{I_{\text{in1}}}^2}{I_1}}$$
$$C\dot{V}_2 = \frac{1}{2}\sqrt{I_o\frac{I_1^2}{I_2}} - \frac{1}{2}\sqrt{I_o\frac{I_{\text{in2}}^2}{I_2}} \quad (10)$$

The left hand sides of (10) represent currents flowing into capacitors of value C connected with voltages V_1 or V_2 across them. The right hand sides of (10) are clearly non-linear, requiring current squaring/dividing and current square-rooting circuits. A high-level block diagram implementation of the square root domain biquad filter is shown in Fig. 3; summing currents at nodes V_1 and V_2 derives the expressions given in (10). The filter cut-off frequency ω_o and quality factor Q can be independently tuned by varying I_o and I_{oq} respectively (the reason for the doubling of the current sources, i.e. $2I_o$ in Fig. 3, will become clear when the full filter implementation is described). The implementation of a square root domain filter thus requires the design of non-linear circuit building blocks, in contrast to conventional IC filter design which is based on the implementation of linear circuit elements such as transconductors. If these non-linear blocks can be designed with good conformity to the required non-linear function over a wide input dynamic range, then square root domain filters may present an attractive alternative to conventional CMOS filter techniques for certain applications.

4. Non-Linear Subcircuit Implementation and Performance

Equations (10) (and Fig. 3) show that, to implement the square root domain biquad, two separate non-linear functions are required. The first is a geometric mean function:

$$I_{\text{out}} = \sqrt{I_x I_y/4} \quad (11)$$

The second function has the form:

$$I_{\text{out}} = \sqrt{\frac{I_x I_y^2}{4I_z}} \quad (12)$$

This second function can be implemented by two subcircuits: a current squarer/divider to implement the function $I_w = ({I_y}^2/I_z)$, followed by a geometric mean circuit to implement $I_{\text{out}} = \sqrt{(I_x I_w/4)}$. The required non-linear functions (geometric mean and current squarer/divider) can be synthesized using the MTL principle, and form the basic building blocks for higher order square root domain filter synthesis [24].

4.1. Geometric Mean Circuit

Consider a four transistor NMOS MTL loop, with M_1, M_2 in a CCW direction and M_3, M_4 in a CW direction. Assuming all devices are matched we can write:

$$\sqrt{I_{\text{d1}}} + \sqrt{I_{\text{d2}}} = \sqrt{I_{\text{d3}}} + \sqrt{I_{\text{d4}}} \quad (13)$$

Define $I_{\text{d1}} = I_x$ and $I_{\text{d2}} = I_y$ as the input currents. If

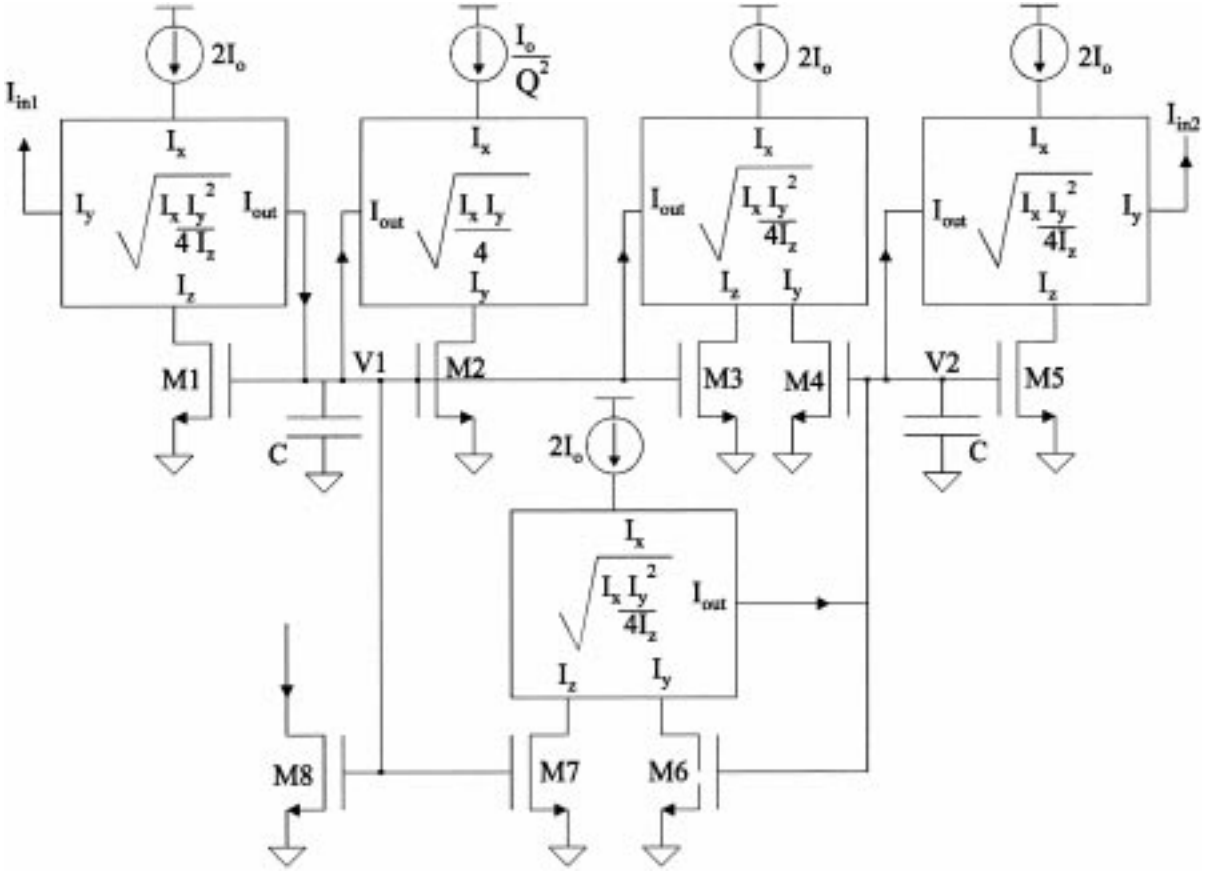


Fig. 3. A block diagram implementation of a square root domain biquad filter.

we ensure that $I_{d3} = I_{d4}$, and define an output current $I_{out} = I_{d4} - (I_x + I_y)/4$, then:

$$I_{out} = \frac{\left(\sqrt{I_x} + \sqrt{I_y}\right)^2}{4} - \frac{I_x + I_y}{4} = \frac{\sqrt{I_x I_y}}{2} \tag{14}$$

The required geometric mean function can thus be implemented by the MTL circuit proposed in [21] and shown in Fig. 4. This is a current-sinking geometric mean circuit; a current-sourcing version could be implemented by using PMOS rather than NMOS devices, or by using an additional inverting current mirror. This circuit is known as a ''stacked'' MTL topology (since M_2 and M_3 are stacked above M_1 and M_4). Fig. 5(a) shows simulation results (solid lines) using Spectre level 15 models from Austria Micro Systems (AMS) 0.8 μm CMOS process, with I_x fixed at the values shown and I_y varying. All MOSFETs

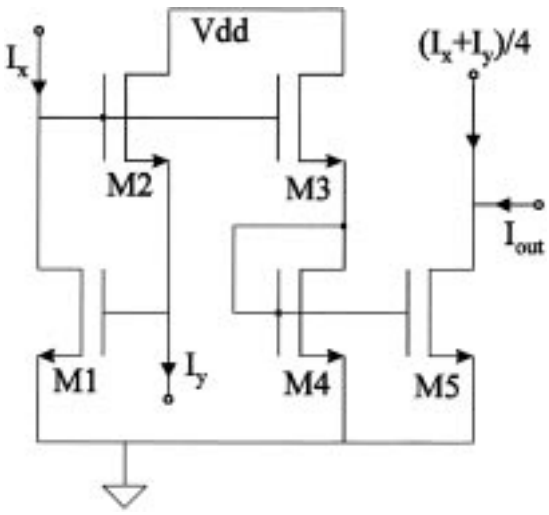


Fig. 4. Geometric mean circuit—a ''stacked MTL'' implementation.

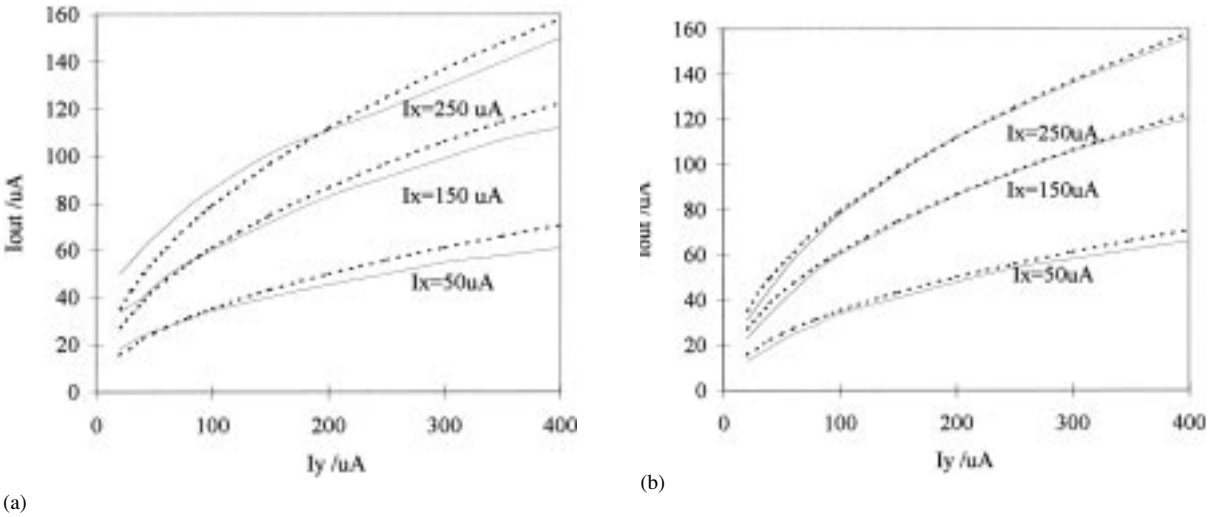


Fig. 5. Comparison of ideal and simulated results for the ''stacked MTL'' geometric mean with (a) body effect included and (b) no body effect.

have an aspect ratio of 12 μm/0.8 μm. The ideal geometric mean characteristics are also shown in dashed lines. The considerable deviation (up to 20% at low current levels) between the ideal and simulated characteristics is due to the body effect ($V_{bs} \neq 0$) causing threshold voltage mismatch, since this is an N-well process and thus all NMOS devices share the same substrate. On a P-well process it would be possible to place each device in a separate well, connecting each source to the well to avoid the body effect. The simulation results in this case are shown in Fig. 5(b), and demonstrate a good conformity with the ideal characteristics over a wide range of input currents, with minimum gate length devices. However the disadvantage of placing each transistor in an individual well is the increase in silicon area, and a reduction in bandwidth due to the large well-substrate capacitance of each individual well.

A better solution is to use an ''up-down'' loop topology such as the example shown in Fig. 2. In this case all devices will have approximately the same source voltage and the body effect is minimized; to further reduce the effect of threshold voltage mismatch, the magnitude of V_{bs} should be made as large as possible. Simulations show that the resulting circuit has good accuracy and wide bandwidth, thus this topology was chosen in all following architectures. However the complexity of the circuit required to provide the correct input currents may be increased when using an up-down topology rather than a stacked loop.

4.2. Current Squarer/Divider Circuit

Bult and Wallinga proposed a current squarer/divider circuit in [14], but since this implementation is based on a stacked loop topology the accuracy is insufficient for our purposes. An up-down loop topology which eliminates the body effect was proposed in [21] and is shown in Fig. 6 (this is a current sourcing circuit; a current sinking version

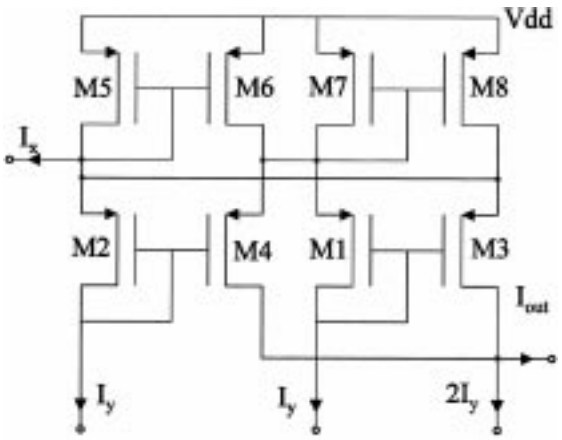


Fig. 6. Current squarer/divider—an ''up-down MTL'' topology.

could be implemented by using NMOS rather than PMOS devices). When all transistors are matched (equal values of β), the MTL expression for the loop can be written as:

$$\sqrt{I_{\mathrm{d1}}} + \sqrt{I_{\mathrm{d2}}} = \sqrt{I_{\mathrm{d3}}} + \sqrt{I_{\mathrm{d4}}} \tag{15}$$

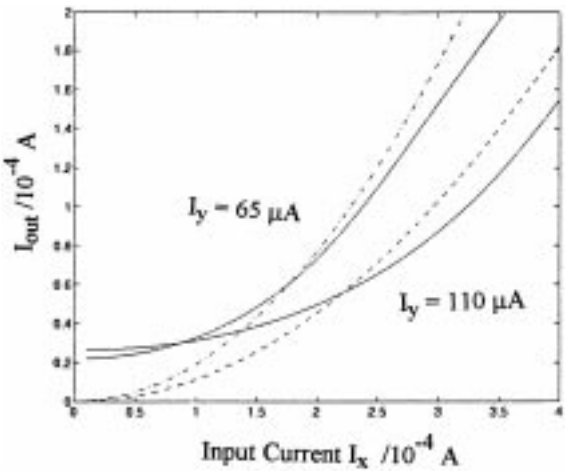
Transistors M_5 and M_6 form a current mirror which ensures $I_x = I_{\mathrm{d4}} - I_{\mathrm{d3}}$. Defining an output current $I_{\mathrm{out}} = I_{\mathrm{d3}} + I_{\mathrm{d4}} - 2I_y$, gives the result:

$$I_{\mathrm{out}} = \frac{I_x^2}{8I_y} \tag{16}$$

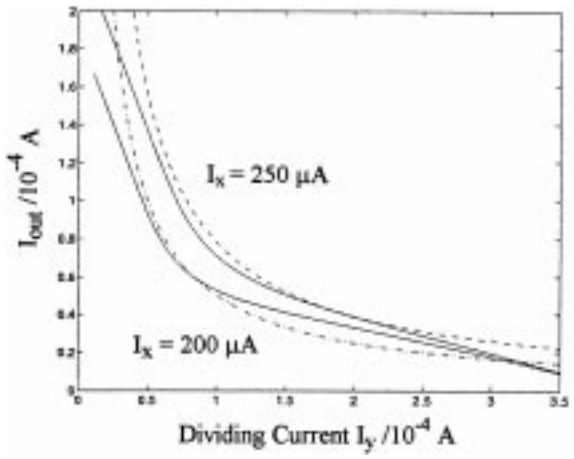
This expression is valid as long as I_{d3} and I_{d4} are greater than zero, i.e.:

$$-4I_y < I_x < 4I_y \tag{17}$$

Fig. 7 shows simulation results for the current squarer/divider circuit using AMS 0.8 μm CMOS technology. All p-channel MOSFETs were implemented with aspect ratio 12.8 μm/0.8 μm, and regulated cascode current sources were implemented to drive the circuit. The circuit was simulated to evaluate both the current squaring and current dividing behavior. Fig. 7(a) shows the simulation results (solid lines) for the current squaring action, with the dividing current I_y held constant at the values shown and input current I_x varying. The ideal characteristics are also shown as dashed lines. The quadratic relationship is clear for input currents in the range given by equation (17); outside of this range the output current increases linearly with the input current. The device dimensions were optimized for input currents around 200 μA. Fig. 7(b) shows the simulation results (solid lines) for the circuit dividing action, with the squaring input current I_x held constant at the values shown and the dividing current I_y varying. Ideal characteristics are again shown as dashed lines. The curves are bounded at the lower end of the range by equation (17). At the upper end, the simulated characteristics are increasingly in error due to mobility reduction effects at higher current levels (discussed below). Because the output current is the difference of two large currents, the relative errors increase at higher current levels. The small-signal bandwidth of the circuit was simulated to be more than 300 MHz; this figure was also confirmed by large-signal transient simulation.



(a)



(b)

Fig. 7. Comparison of ideal ans imulated results for the current squarer/divider circuit demonstrating (a) the current squaring action and (b) current dividing action.

4.3. Sub-Circuit Performance Limitations

Errors in the sub-circuit performance due to the body effect have already been mentioned, and can be minimized by selecting an up-down loop topology. Other second order effects which are likely to affect circuit performance include mobility reduction, channel-length modulation, and threshold voltage mismatches. These issues will be discussed briefly below in relation to the current squarer/divider circuit of Fig. 6, but similar comments will apply to the

geometric mean circuit (and indeed, to other similar MTL circuit structures).

Mobility Reduction. As the transverse electric field along the channel (E_x) increases in magnitude, the mobility of carriers in the channel decreases. There are several models of mobility versus electric field; one particular relation which is commonly used is [23]:

$$\mu = \frac{\mu_{\text{eff}}}{\left(1 + \left(\frac{\mu_{\text{eff}} E_x}{\nu_{\text{sat}}}\right)^2\right)^{1/2}} \tag{18}$$

where μ_{eff} is the effective carrier mobility for small transverse fields, ν_{sat} is the saturation velocity and E_x is the electric field strength along the channel. Assuming that the device is in saturation, the transverse field strength E_x will be proportional to $(V_{gs} - V_{th})$. For an approximate analysis it is often sufficient to simplify equation (18) to a first order expression [22]:

$$\mu = \frac{\mu_{\text{eff}}}{1 + \theta(V_{gs} - V_{th})} \tag{19}$$

where θ is a mobility reduction parameter. Referring to Fig. 6, writing the MTL equation for the loop:

$$\sqrt{4I_y} = \sqrt{\frac{1 + \theta(V_{gs3} - V_{th})}{1 + \theta(V_{gsy} - V_{th})}}\sqrt{I_{d3}} + \sqrt{\frac{1 + \theta(V_{gs4} - V_{th})}{1 + \theta(V_{gsy} - V_{th})}}\sqrt{I_{d4}} \tag{20}$$

where V_{gsy} is the gate-source voltage of transistors with a drain current I_y.

Substituting $V_{gs} - V_{th} = \sqrt{(I_d/\beta)}$, equation (20) is thus rewritten as:

$$\frac{1 + \theta\sqrt{I_{\text{d3}}/\beta}}{1 + \theta\sqrt{I_y/\beta}} I_{\text{d3}} + \frac{1 + \theta\sqrt{I_{\text{d4}}/\beta}}{1 + \theta\sqrt{I_y/\beta}} I_{\text{d4}} = 2Iy + \frac{\left(\frac{1 + \theta\sqrt{I_{\text{d4}}/\beta}}{1 + \theta\sqrt{I_y/\beta}} I_{d4} - \frac{1 + \theta\sqrt{I_{\text{d3}}/\beta}}{1 + \theta\sqrt{I_y/\beta}} I_{\text{d3}}\right)^2}{8I_y} \tag{21}$$

Assuming that the left hand side of equation (21) is relatively constant, and defining $I_{\text{out}} = I_{d3} + I_{d4} - 2I_y$ as previously, gives the result:

$$I_{\text{out}} = \frac{\left(1 + \frac{3}{2}\theta\sqrt{I_y/\beta} I_x\right)^2}{8\left(1 + \theta\sqrt{I_y/\beta}\right)^2 I_y} + \frac{\left(1 + \frac{3}{2}\theta\sqrt{I_y/\beta}\right)\theta\sqrt{Iy/\beta} {I_x}^4}{128\left(1 + \theta\sqrt{I_y/\beta}\right)^2 {I_y}^3} + \frac{\theta^2 {I_x}^6}{8192\beta\left(1 + \theta\sqrt{I_y/\beta}\right)^2 {I_y}^4} \tag{22}$$

The output will contain fourth and sixth order terms in I_x, as well as third and fourth order terms in I_y. The fundamental of the output (i.e. ${I_x}^2/8I_y$ term) will also be modulated by a weak function of I_y.

By simple curve fitting to the simulated characteristics, the mobility reduction parameter is found to be about 0.07 for the AMS 0.8 μm CMOS technology. With this value of θ, simulations show that the error in the fundamental term is relatively unaffected by changes in I_y, shifting from 2.5% to 2.8% above the ideal value when I_y is varied between 1 and 100 μA. For a practical range of input currents, the deviation from the ideal response due to fourth order components of I_x is found to be less than -40 dB. The sixth order deviation is less than -80 dB, and is unlikely to be of any great significance.

Channel Length Modulation. The variation of channel length with changes in V_{ds} is generally modeled by the equation:

$$I_{\text{d}} = \beta(V_{gs} - V_{th})^2(1 + \lambda V_{\text{ds}}) \tag{23}$$

where λ is the channel length modulation parameter. In Fig. 6, the diode-connected devices M_1 and M_2 have $V_{ds} = V_{gs}$, thus channel length modulation will be minimal. Considering the effect of devices M_3 and M_4, the output current can be recalculated as:

$$I_{\text{out}} = \frac{\left(\frac{I_{\text{d3}}}{1 + \lambda V_{\text{ds3}}} - \frac{I_{\text{d4}}}{1 + \lambda V_{\text{ds4}}}\right)^2}{8I_y} \tag{24}$$

assuming that the sum $I_{\text{d3}} + I_{\text{d4}}$ is largely unaffected by channel length modulation effects. With typical operating voltages, the simulated deviation from the ideal characteristic due to channel length modulation is small (less than -80 dB for most of the operating range).

Threshold Voltage Mismatch. Assuming that devices $M_5 - M_8$ are matched, any mismatch in the threshold voltages of $M_1 - M_4$ will cause an offset in the MTL loop equation as follows:

$$\sqrt{\frac{4I_y}{\beta}} + \sum_{i=1}^{4} \Delta V_{thi} = \sqrt{\frac{I_{\mathrm{d3}}}{\beta}} + \sqrt{\frac{I_{\mathrm{d4}}}{\beta}} \tag{25}$$

where

$$\sum_{i=1}^{4} \Delta V_{thi} = \Delta V_{th1} + \Delta V_{th2} - \Delta V_{th3} - \Delta V_{th4} \tag{26}$$

Threshold voltage mismatches are represented by a deviation from a mean value V_{tho}, i.e. $V_{th} = V_{tho} + \Delta V_{thi}$. The effect of threshold voltage mismatches on the circuit of Fig. 6 can be calculated as:

$$I_{\mathrm{out}} = \frac{I_x^2}{8I_y} - \frac{I_x^2}{8I_y^{3/2}} \left(\sum_{i=1}^{4} \Delta V_{thi} \right) + 2I_y^{3/2} \left(\sum_{i=1}^{4} \Delta V_{thi} \right) \tag{27}$$

The threshold voltage mismatch will not cause any deviation proportional to I_x, but will create new terms proportional to ${I_y}^{-3/2}$ and $I_y^{3/2}$. These ''fractional harmonics'' are a result of the non-linear signal processing within square root domain filters, and are not generally encountered in conventional linear filters.

MOSFET Square Law Deviation. At this point it is instructive to examine whether the MOSFET square law approximation is a valid one. In the relevant literature it has been shown that, for long channel MOSFETS, the square law approximation agrees with experimental results to a great extent [22,23]. However these assumptions may no longer apply to modern technologies which have increasingly smaller geometries, driven by power consumption, speed and silicon area considerations.

A reduction in the gate length increases the importance of second-order ''short channel'' effects in the MOSFET characteristic, such as channel length modulation, mobility reduction, and velocity saturation. Channel length modulation and mobility reduction have been briefly discussed above. For shorter channel lengths, the increasing transverse electric field in the channel further modulates the carrier mobility causing the velocity of the carriers in the channel to saturate. This velocity saturation has two main effects:

- The drain current is scaled by a factor $(1 + V_{ds}/(1 + LE_c))^{-1}$ (i.e. reduced), where E_c is the critical transverse field strength.
- At very short gate lengths it will destroy the square law relationship, and leads to a linear dependence between drain current and gate-source voltage.

A minimum gate length which largely avoids short channel effects due to mobility reduction and velocity saturation can be determined by referring to equation (19). To ensure that mobility stays approximately constant with changes in transverse electric field, we require:

$$\frac{\mu_{\mathrm{eff}} E_x}{\nu_{\mathrm{sat}}} < 1 \tag{28}$$

Assuming $E_x = (V_{gs} - V_{th})/L$, a minimum gate length can be approximated as:

$$L_{\mathrm{min}} > \frac{\mu_{\mathrm{eff}}(V_{gs} - V_{th})}{\nu_{\mathrm{sat}}} \tag{29}$$

With typical values $\nu_{\mathrm{sat}} = 10^7\,\mathrm{cm/s}$ and $\mu_{\mathrm{eff}} = 500\,\mathrm{cm}^2/\mathrm{s}$ we obtain the result:

$$L_{\mathrm{min}} > \frac{(V_{gs} - V_{th})}{2}\,\mu\mathrm{m} \tag{30}$$

This minimum gate length will ultimately limit the maximum operating frequency of square-root domain filters.

5. Filter Implementation

5.1. Implementation

Returning to the biquad filter circuit of Fig. 3, we are now able to implement a full transistor level circuit by replacing the high-level non-linear blocks with the geometric mean and current-squarer divider circuits shown in Sections 4.1 and 4.2. The blocks with current-sourcing outputs are implemented by PMOS MTL circuits, while blocks with current-sinking outputs are implemented by NMOS MTL circuits. Aspect ratios of MOSFETs M1-M8 in Fig. 3 are equal to 16 μm/1.2 μm. The bias currents I_o are used to tune the filter cutoff frequency ω_o, while the quality factor Q is set by bias current $I_{oq} = I_o/Q^2$. Referring to equation (10), terms of the form $\sqrt{(I_o I_x^2/I_y)} = \sqrt{(I_o I_w)}$ need to be

generated. The output from the current squarer/divider circuit is $I_x^2/8I_y$, and so needs to be multiplied by eight before processing by the geometric mean circuit. In practice a current mirror of 1:4 ratio is used to multiply this current by four, while the tuning current term I_o is multiplied by two, to achieve the same net effect. This has the further advantage of ensuring that the input currents to the geometric mean circuit are of similar magnitude, thus reducing the output error (see Fig. 5(a)). In addition, the DC levels of the input currents are scaled so that $I_{u1} = (1 + 1/Q)I_{u2}$ to ensure a stable equilibrium condition at DC [6].

The level of distortion at the output is related to the magnitude of the voltage swings across the capacitors. The minimum and maximum capacitor voltages are restricted by the strong inversion condition and the mobility degradation respectively. Thus the gate-source voltage of transistors connected to the capacitor nodes ($M_1 - M_8$ in Fig. 3) must be limited to between approximately $(V_{th} + 0.1\,\text{V})$ and $(V_{th} + 0.6\,\text{V})$ for this technology to prevent excessive output distortion. Although this factor may seem to limit the usefulness of square-root domain circuits, it must be remembered that capacitor voltages are a compressed (square-rooted) version of the circuit currents, and excessive output distortion does not arise until the input current modulation is higher than about 80%.

5.2. *Performance Analysis*

The circuit was simulated using device parameters from the AMS 0.8 μm CMOS process; large signal transient simulations were performed at a range of frequencies to confirm the response obtained from AC (small-signal) analysis. Applying a signal at I_{in2} gave a lowpass response much as expected, although ω_o and Q were shifted slightly from the ideal design values calculated using the expressions derived in Section 3. With $C = 20\,\text{pF}$, $I_o = 120\,\mu\text{A}$ and $I_{oq} = 100\,\mu\text{A}$ the ideal calculated values for f_o and Q were 3.75 MHz and 1.1 respectively, while the values obtained from simulation were 3.9 MHz and 0.9. Similarly with $I_o = 180\,\mu\text{A}$ and $I_{oq} = 150\,\mu\text{A}$ the ideal values of f_o and Q were calculated as 4.59 MHz and 1.1 respectively, while the values obtained from simulation were 4.77 MHz and 0.9.

The bandpass response obtained by applying an input signal at I_{in1} showed a similar shift in the simulated values of f_o and Q. However a more serious deviation from the ideal response was seen in the bandpass case, in that the low frequency attenuation was severely degraded. To develop insight into the source of the filter non-idealities, the state equations of the filter were re-derived from the block diagram of Fig. 3, this time including two additional resistors R_1 and R_2 connected in parallel with the integrating capacitors at nodes V_1 and V_2 respectively. R_1 and R_2 represent the total output impedance of the geometric mean and current squarer/divider circuits at these nodes; in practice, these values will be dynamic (large signal resistances). Considering the non-linear geometric mean and current squarer/divider sub-blocks to have ideal responses, the state equations are modified by the presence of R_1 and R_2:

$$2C\sqrt{\beta I_1}\dot{V}_1 + 2\frac{\sqrt{\beta I_1}}{R_1}V_1 = -\frac{C\omega_o}{Q}I_1 - C\omega_o I_2 + C\omega_o I_{\text{in1}}$$

$$2C\sqrt{\beta I_2}\dot{V}_2 + 2\frac{\sqrt{\beta I_2}}{R_2}V_2 = C\omega_o I_1 - C\omega_o I_{\text{in2}} \qquad (31)$$

Applying the mappings for I_1 and I_2 as given in equation (8), these state equations are modified to:

$$\dot{I}_1 = -\left(\frac{\omega_o}{Q} + \frac{2}{CR_1}\right)I_1 - \omega_o I_2 + \omega_o I_{\text{in1}} - \sqrt{I_1}\left(\frac{2V_T\sqrt{\beta}}{CR_1}\right)$$

$$\dot{I}_2 = I_1\omega_o - \left(\frac{2}{CR_2}\right)I_2 - \omega_o I_{\text{in2}} - \sqrt{I_2}\left(\frac{2V_T\sqrt{\beta}}{CR_2}\right) \qquad (32)$$

These state equations are no longer linear, but contain terms of the form $\sqrt{I_1}$ and $\sqrt{I_2}$. If for the moment we assume that these non-linear terms are very small and can be neglected, equation (32) can be rewritten as:

$$\dot{I}_1 = -I_1\left(\frac{\omega_o}{Q} + \frac{2}{CR_1}\right) - I_2\omega_o + I_{\text{in1}}\omega_o$$

$$\dot{I}_2 = I_1\omega_o - I_2\left(\frac{2}{CR_2}\right) - \omega_o I_{\text{in2}} \qquad (33)$$

Combining these two linear state equations and gives the resulting response:

$$\frac{I_{\text{out}}(s)}{I_1(s)} = \frac{\omega_o I_{\text{in1}}(s + 2/CR_2) + \omega_o I_{\text{in2}}}{s^2 + (\omega_o/Q + 2/CR_1 + 2/CR_2)s + (\omega_o^2 + 4/C^2R_1R_2)} \qquad (34)$$

Compared to the ideal response (equations (6) and

(10)), the cut-off frequency and quality factor are both modified:

$$\omega_o' = \omega_o\sqrt{(1+4/C^2R_1R_2\omega_o^2)}$$

$$Q_o' = Q_o\frac{\sqrt{(1+4/C^2R_1R_2\omega_o^2)}}{1+(2Q_o(R_1+R_2)/\omega_oCR_1R_2)} \qquad (35)$$

In addition, the bandpass zero is shifted up in frequency from zero to $\omega_z = 2/CR_2$.

This approximate linearized analysis predicts that the finite output impedance of the non-linear sub circuits will cause a shift in the expected transfer function. This effect is further illustrated in Fig. 8, which shows simulation results for the bandpass response in which behavioral models were used to represent current squarer/divider and geometric mean circuits. The impedances R_1 and R_2 were assumed to be equal and were varied between 100 kΩ and 1 MΩ in 300 kΩ steps. The increased attenuation with increasing impedance levels is clearly seen, and suggests that an improvement in performance could be obtained by implementing subcircuit designs featuring very high output impedance.

The non-linear terms introduced into the state equations (equation (32)) will introduce ''sub-harmonic'' non linear terms into the output, similar to those of equation (22). These additional harmonic terms can be minimized by minimizing the values of $V_{th}\beta^{1/2}/CR_1$ and $V_{th}\beta^{1/2}/CR_2$.

5.3. *Measured Results*

The biquad filter circuit of Fig. 3 was implemented using AMS 0.8 μm CMOS technology, and a chip photograph is shown in Fig. 9. The circuit was powered from a 5 V power-supply, and CCII-01 current-conveyor amplifiers[1] were used as high-frequency transconductors to convert input signal voltages to currents required at the input of the test circuit. Output currents were measured using a Tektronix CT-2 current probe having a −3 dB bandwidth of 1 GHz. Fig. 10 compares the measured (solid lines) and simulated (dashed lines) bandpass frequency responses for two different values of tuning currents. In the first case (1), $I_o = 120\,\mu$A and $I_{oq} = 100\,\mu$A (i.e. $f_o = 1.9$ MHz and $Q = 1.1$). The input signal was an AC current of 120 μA pk on a DC level of 250 μA. In the second case (2), $I_o = 50\,\mu$A and $I_{oq} = 40\,\mu$A (i.e. $f_o = 1.1$ MHz and $Q = 1.1$). The input signal was an AC current of 50 μA pk on a DC level of 100 μA. Fig. 10 shows that in both cases the simulated and measured results are fairly close, and the difference is likely to be due to processing tolerances (variations in C, β etc.). The low frequency attenuation is almost completely destroyed due to the finite output impedance of the MOSFETs, as described in Section 5.2. The finite output impedance also shifts the bandpass zero up in frequency, and from Fig. 10 the position of this zero is around 500 kHz, which from the approximate analysis of

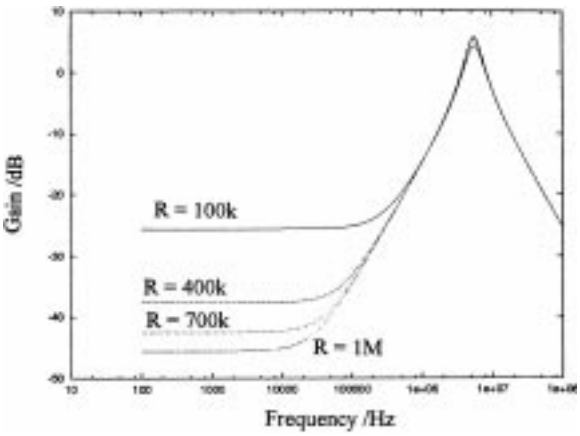


Fig. 8. Simulation results of a behavioral model of the biquad filter, demonstrating the degradation in stopband attenuation with decreasing sub-circuit output resistance.

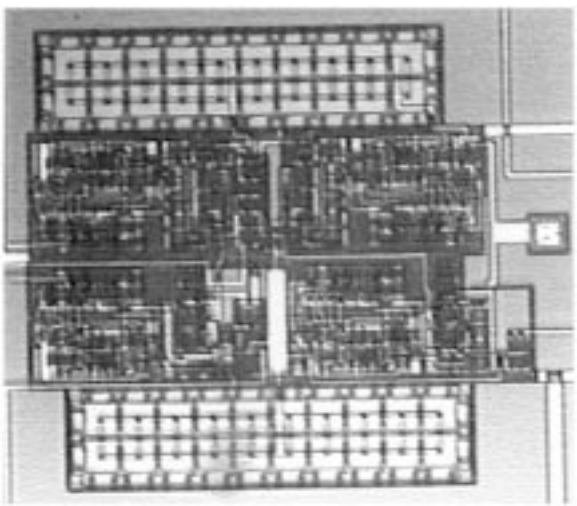


Fig. 9. Micophotograph of the biquad filter.

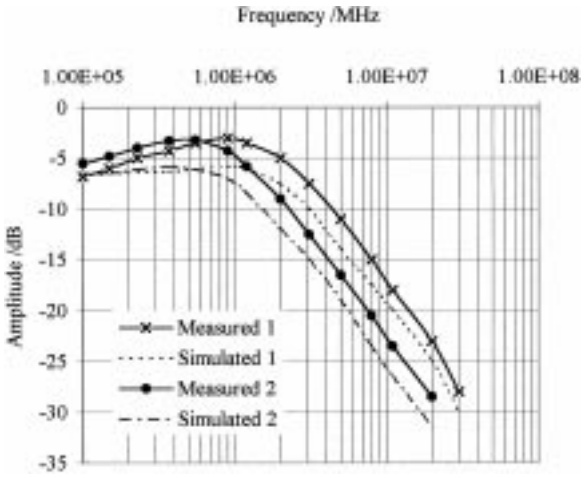


Fig. 10. Comparison of simulated and measured biquad bandpass response.

Section 5.2 predicts an impedance R_2 of around 40 kΩ shunting the capacitor at node V_2. This conclusion also seems to be confirmed by reference to Fig. 8.

For the tuning and input current levels given in (1), and with input signal frequency at 100 kHz, the second and third harmonics were measured as − 50 dB and − 54 dB relative to the fundamental, respectively. Higher order harmonics were below the noise floor at − 57 dB. In addition, additional frequency terms occurring between the integer harmonics were observed. For an input signal of 100 kHz, the following spectral components were also observed (levels relative to the fundamental):

Table 1. Measured harmonic components.

Frequency/kHz	Signal Level/dB
144.6	– 54.8
153.4	– 54.4
183.0	– 55.2
229.4	– 56.0

The exact cause of these additional spectral terms is not entirely clear but is undoubtedly due to the internally non-linear operation of the circuit. Interfering frequencies coupling into the circuit are likely to combine with input signal harmonics within the non-linear sub circuits, causing spurious tones at the output. In addition, mismatch errors and finite output impedance cause deviations in the subcircuit response as discussed in Sections 4.3 and 5.1, which also leads to non-exact cancellation of the harmonic terms generated internally as part of the non-linear signal processing.

6. Conclusions

This paper has outlined the CMOS square root domain filter synthesis methodology, and has described the implementation of particular non-linear subcircuits. Although the circuit designs presented in this paper verify the methodology presented, the potential for performance improvement is clearly apparent and will be the subject of future investigation. The current squarer-divider implementation shown here causes the greatest deviation from the ideal response, and alternative circuit topologies may prove more suited to this application. However the authors believe that the results presented are encouraging, in that they demonstrate the validity of the proposed approach as well as providing avenues for future research in this area.

Note

1. Courtesy of LTP Electronics, Oxford, UK.

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