Differential Drive CMOS Rectifiers for RF Energy Harvesting

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Abstract

In this work, we review the design fully-differential RF-DC rectifiers in the context of the design of CMOS passive UHF RFID transponder integrated circuits. The results are applicable to the systems where the supply voltage is obtained by extracting ambient RF energy. The operation of the fully-differential rectifiers is explained starting from a simple diode-C rectifier circuit. It is shown that fully differential-rectifiers are extension of the basic rectifier circuit where the 2-terminal diodes are replaced by 3-terminal MOSFETs allowing the reduction of the voltage across the switches. We also review the design of the cascaded multi-stage rectifiers from the perspective of a circuit design engineer to yield some design guidelines when designing such circuits.

We propose a novel methodology for the quick and correct determination of the input impedance of passive RFID circuits by shooting-newton type simulations including in the input power levels where the input port's current-voltage relationship is strongly non-linear.The results should be applicable to other circuits where the relationship between voltage across the input port and input terminal currents are strongly non-linear.

Chapter 1

Single- and multi-stage CMOS RF-DC Rectifier Design

INTRODUCTION

RF-DC rectifiers are one of the fundamental building blocks of any electronic system that harvests the ambient RF power to supply the rest of the circuitry. One of the best known examples of the such energy harvesting systems are the UHF radio frequency ID (RFID) transponder chips. Another up and coming application area is the wireless charging circuits for the ubiquitous mobile devices. In this work, we will concentrate on the requirements of the UHF RFID transponder chips. However the discussion is equally applicable to other types of circuits utilizing RF energy harvesters.

Passive UHF RFID transponders need to obtain their operating power from the RF signals emitted by an RFID reader. It is quite probable that the such devices could use RF power at the adjacent bands, for example 900 MHz GSM bands. We will discount these possibilities as they have not been proven to be a reliable source of RF power so far. UHF RFID readers have statuary restrictions on the emitted RF power. For example, the European standards limit the emitted RF power approximately to 2 W ERP, while the USA limit is the double of this figure, i.e. 4 W EIRP [1].

State-of-the-art RFID transponder circuits work with input RF power levels as low as

-18dBm, equivalent to less than 20 µW [2]. Even assuming that the input RF power is perfectly converted to the DC power by the rectifier and the chip has a single supply voltage of 1 V, the chip's current drain has to be kept below 20 µA. The RFID reader normally transmits various commands to the transponder using ASK modulation further limiting the average RF power available to the RFID transponder. Thus, these chips are severely limited by the available RF power and would need highly efficient RF-DC rectifiers to extend their reading range.

The figure of merit for RF-DC rectifiers are the Power Conversion Efficiency (PCE) number. *Power conversion efficiency* is the ratio of the output DC power to the input RF power and is always less than one. We could express the PCE as

$$\text{PCE} = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} < 1 \tag{1.1}$$

To increase PCE, we need to minimize the P_{loss}. In the following section, we will look into the operation of RF rectifiers and the possible causes of power losses in the rectifier circuit.

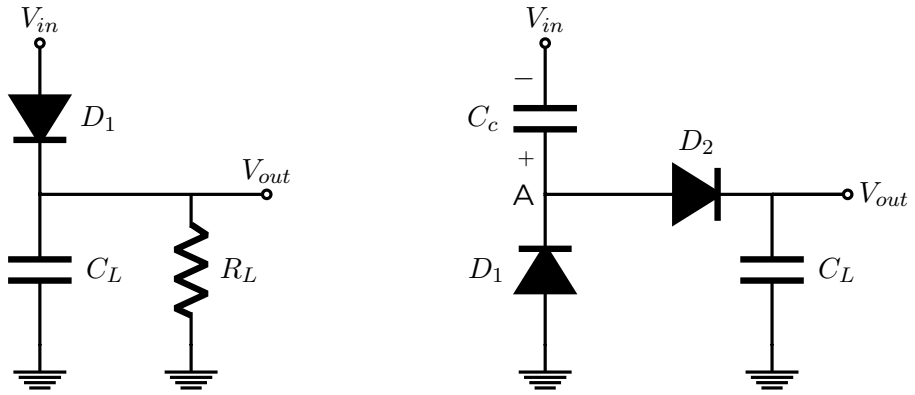
RECTIFIER CIRCUITS

DIODE-C RECTIFIER

The simplest RF-DC rectifier is a diode-capacitor circuit shown in figure 1.1a. Assume that the output voltage, V_{out} is at ground potential at $t = 0$, i.e. $V_{out}(0) = 0$ and the amplitude of the input signal, $V_{in,pk}$ is larger than the diode turn-on voltage, i.e. $V_{in,pk} > V_{on}$. At every period of the V_{in}, the load capacitor, C_L, will be charged until $V_{\text{out}} = V_{in,pk} - V_{on}$.

The diode-C rectifier suffers from the fact the output voltage is always at least one diode turn-on voltage, V_{on} lower than the $V_{in,pk}$. Reduction of V_{on} by the use of the Zener diodes is not always an option in modern CMOS fabrication technologies.

R_L represents the current drawn by the rest of the circuitry which the rectifier supplies. It is an approximation as the the voltage-current characteristics of the load cir-



(a) Diode-C RF-DC rectifier. (b) Voltage Doubler Circuit.

Figure 1.1: Diode-C and its extension, Voltage-Doubler, circuits.

cuit looking into its supply terminal is probably much more complex and is likely to be nonlinear. As the load capacitance is charged only in a portion of the input signal period, V_{out} will fluctuate over the time when D1 is off with a time constant of $\tau = R_L C_L$.

VOLTAGE DOUBLER

To increase the output voltage further, the voltage doubler circuit (figure 1.1b) has been regularly used (see figure 1.1b). The voltage-doubler circuit can be thought of an extension of diode-C rectifier circuit where an additional mirror-image of diode-C rectifier is added before it (compare node V_{in} in figure 1.1a with node Ⓐ in figure 1.1b).

Assume that the V_{in} has an amplitude of $V_{in,pk}$ in figure 1.1b. When the input voltage V_{in} is below the ground potential by V_{on}, D1 diode is turned on. Thus, the coupling capacitor C_c is charged to $V_{in,pk} - V_{on}$ with the polarity shown. As the input voltage starts increasing after reaching its nadir at $-V_{in,pk}$, the $D1$ diode would immediately *turn off* as the voltage across it will be now less than V_{on}[1]. When the voltage at node A is higher than the turn-on voltage of the diode D_2, D_2 will start conducting. As the input voltage reaches its positive peak at $V_{in,pk}$, the potential at node Ⓐ reaches $V_{in,pk} + V_{in,pk} - V_{on}$, where we assumed that V_{out} is initially at ground potential, i. e. 0V.

[1]We assume here that the diode has ideal V-I characteristics with a well-defined turn-on voltage of V_{on}

The load capacitance, C_L will be charged until the voltage across it reaches

$$V_{in,pk} + V_{in,pk} - V_{on} - V_{on} = 2 \cdot (V_{in,pk} - V_{on}) \tag{1.2}$$

The process of V_{out} reaching its steady-state voltage level could take many cycles of V_{in}. When the steady-state is reached, V_{out} should be constant if the reverse leakage currents of the diodes are ignored. The reverse leakage currents would be discharging the load capacitance between two maximums of the input voltage at the beginning and at the end of the input signal's period. Therefore, the output voltage will *droop* during this time, and it would be recharged to its peak value when D2 is conducting. Limiting the reverse leakage current over process and temperature variations is one of the significant challenges of the RF-DC rectifiers.

The other significant challenge is due the effect of the value of V_{on} at the V_{out}. The load capacitor C_L cannot be charged at all if $V_{in,pk} < V_{on}$ holds.

SINGLE-ENDED CMOS RECTIFIER

We can think of a diode as a switch whose conduction state, i. e. whether there is high or low impedance between its terminals, is determined by the voltage across its terminals. Of course, we know a better option for switches, allowing more flexibility in controlling the impedance between the switches two terminals, i. e. transistors. MOSFETs are especially suited to be used as switches, as they need no current in their control terminals, i. e. gate terminals.

Starting with this idea, let's change all the diodes in the voltage-doubler circuit (figure 1.1b) to the NMOS transistors for the moment resulting in the circuit schematic shown in figure 1.2.

When $V_{in} < 0$ M1 should be conducting, i.e. *on*, while M2 should be off. Thus, potential at G1 node should be held high, while the potential at G2 node should be low. When the $V_{in} > 0$ holds, M1 should be off, while M2 should be on. Thus, G1 should be held low, while G2 should be high. We could summarise the foregoing the discussion in table

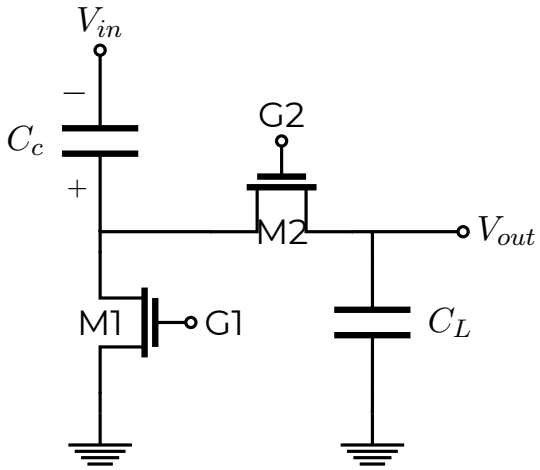


Figure 1.2: MOSFET based voltage-doubler circuit.

$\mathbf{V}_{in}$	G1	G2	M1	M2
low	high	low	on	off
high	low	high	off	on

Table 1.1: Input signal, gate voltages and transistor states for the NMOS based voltage-doubler circuit.

As could be seen in table **??**, the potentials of nodes G1 and G2 must be opposite of opposite polarities if both switches were to realised using NMOS transistors. If we were to replace M2 by a PMOS device, both G1 and G2 nodes could have the same polarity. The resulting circuit is shown in figure 1.3.

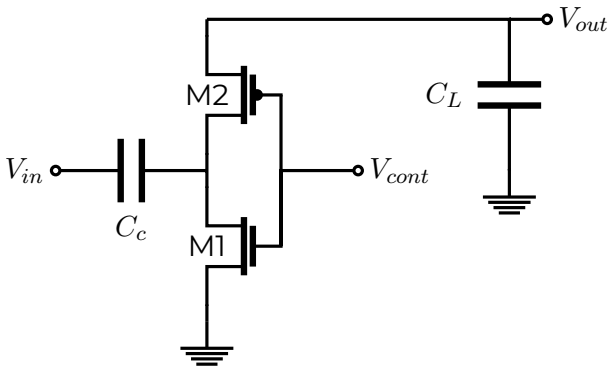


Figure 1.3: Final version of the MOSFET single-ended rectifier circuit.

The gate voltages and switch states for this new circuit is summarized in the table 1.2:

V_{in}	G1	G2	M1	M2
low	high	high	on	off
high	low	low	off	on

Table 1.2: Input signal, gate voltages and transistor states for the single-ended CMOS rectifier.

The drain-to-source voltages, (V_{DS}) of M1 and M2 will not be identically zero when they are conducting current. However, their V_{DS} could be made much smaller than a silicon diode, comparable to a Schottky diode. By adjusting the aspect ratio of the M1 and M2, the value of V_{DS} for M1 and M2 could be much better controlled and reduced compared to a standard diode in a CMOS process. On the other hand, the leakage currents could be problematic in the process technologies with sub-100 nm feature sizes.

DIFFERENTIAL-DRIVE CMOS RECTIFIER

The next step is realisation of the gate voltages for M1 and M2 for the MOSFET based voltage-doubler circuit. It could be seen from the table 1.2 that V_{in} and V_{cont} should be of opposite polarities. To obtain the anti-phase V_{cont} signal, we need to reexamine the incoming RF signals in a RFID tag.

A passive RFID tag has two symmetric terminals constituting a port connected to a dipole antenna as shown in figure 1.4. The RFID tag antenna converts incident RF electromagnetic waves into voltages[2] at its output port [**Grosinger2010**, 1]. One very common technique in the design of RFID rectifiers to connect one of the antenna terminals to the substrate of the die (normally p-type) and regard it as the ground node. This assumption is not strictly correct as the chip substrate is not really connected to a solid ground potential. Tag antenna and transponder chip are typically insulated.

The RF signal at the output of a symmetric antenna is in fact differential. Therefore, the control voltage, V_{cont} in figure 1.3, could be supplied by the anti-phase signal in the

[2] and currents.

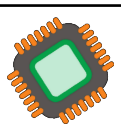


Figure 1.4: A typical UHF RFID tag with meandered dipole antenna

output port of the antenna. We can now construct a full-differential rectifier where the each half circuit supplies current to the output load once in each period of the input RF signal. The differential-drive CMOS rectifier designed by the preceding arguments is shown in figure 1.5.

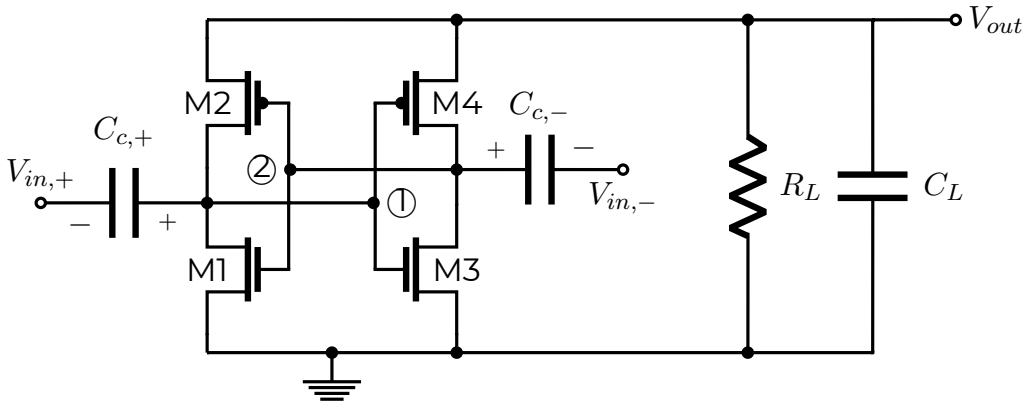


Figure 1.5: Differential Drive CMOS Rectifier Circuit

We could also view this circuit as a cross-coupled inverter pair:

- 1st inverter (M1 and M2)
- 2nd inverter (M3 and M4)

We could understand the operation of this circuit by analysing the circuit for the opposite polarities of the input differential signal at the steady-state:

1. When $V_{in,+}$ is high, $V_{in,-}$ is low, the potential of the node ① is at $2 \cdot V_{in,pk} - V_{DS,1}$, while the voltage at the node ② goes as low as $V_{DS,3}$.
2. Conversely, when $V_{in,-}$ is high, $V_{in,+}$ is low, the potential of the node ② is at $2 \cdot V_{in,pk} - V_{DS,4}$, while the voltage at the node ① goes as low as $V_{DS,1}$.

Ignoring the effect of the load resistance, R_L, the steady-state value of the output voltage for the differential-drive CMOS voltage-doubler circuit is:

$$V_{out} = 2 \cdot V_{in,p} - V_{DS,1} - V_{DS,2} \tag{1.3}$$

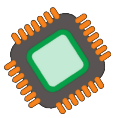
where we assumed The positive feedback action due to two cross-coupled inverters help the switches to change their state quickly reducing the duration when both NMOS and PMOS devices in an inverter are active. During this period, the charge on the load capacitance would be discharged to ground (substrate).

Viewing the differential-drive CMOS rectifier as a cross-coupled inverter helps us in correcting a misnomer in Kotani et. al. work[3], where it is stated that

> "...we propose an "active" Vth cancellation scheme in which Vth can be minimized in a forward bias condition and be increased in a reverse bias condition automatically by a cross-coupled differential circuit configuration."

There is no V_{th} cancellation as the switching elements are no longer the diodes where the voltage across the diode has to be larger than the V_{th} in order to switch it conducting state. Instead the switching elements' states are controlled by a third terminal, i.e. their gates. If the MOSFET's $|V_{GS}|$ is less than $|V_{th}|$ then the device is OFF, i.e. non-conducting. If the reverse is true, then the device is ON, i.e. it conducts current.

Increasing the *the gain of the inverters* would reduce the total charge conducted from the load capacitance to the ground by reducing the duration when both transistors (NMOS and PMOS) along the current path are in active or linear region of operation depending on the voltage across C_L. We have to remember that the output voltage of the rectifier could be quite low when the rectifier is most sensitive to the design parameters, i.e. when input RF power is low. Therefore the NMOS and PMOS devices will be in subthreshold region of operation.



SIMULATION RESULTS

In this section, some simulation results for a single-stage rectifier[3] will be presented. The chosen process technology is TSMC 180nm MS/RF technology but no native or low-V_{th} transistors are used in the design. However the process offers MIMCAPs with 2fF/μm^2 capacitance density. MIMCAPs are used for RF signal coupling and to store the charge at the output of the rectifier.

The design was not extensively optimized for maximum PCE and output voltage, but is presented to discuss the performance parameters of the CMOS differential-driver rectifier circuit. The table 1.3 show the dimensions of the transistors in the design (please refer to figure 1.5).

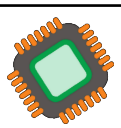
	M1	M2	M3	M4
W	2 µm	4 µm	2 µm	4 µm
L	180 nm	180 nm	180 nm	180 nm

Table 1.3: The transistor gate widths and lengths for the presented CMOS differential drive rectifier.

The coupling capacitors (C_c in figure 1.5) are chosen to be quite small, 0.2 pF. The larger coupling capacitor values will give higher values of PCE and conseqently, but a cost of making the finaly layout area of the circuit the larger. The parasitics due to the bottom plate of MIMCAPs will also increase leading to diminishing returns with increasing coupling capacitor values. We model the load presented by the rest of circuitry on chip, we used a load resistance of 50 kΩ as indicated in figure 1.5 by R_L. The value of the load resistor will affect the PCE and output voltage simulations. We assume that this value to be reasonable approximation as a typical UHF RFID circuit will draw around 20 µA when supplied by a 1 V voltage supply.

First simulation results presented here concerns the output voltage of the rectifier for different RF input power levels as shown in figure 1.6. Input frequency is held at 880 MHz . It must be noted the input RF power levels of the rectifier presented in these simulations are not the magnitude of the RF power output of a *port* element in

[3] We will discuss the multi-stage rectifiers in the next section.



the simulator. The power levels for the port indicated in the simulator are only correct when the load of the RF power source is matched to the source impedance of the *port* element, usually 50 Ω. Here the input impedance of the rectifier is certainly not equal to 50 Ω and actually changes with the applied input RF power level in a non-linear manner [4, 5].

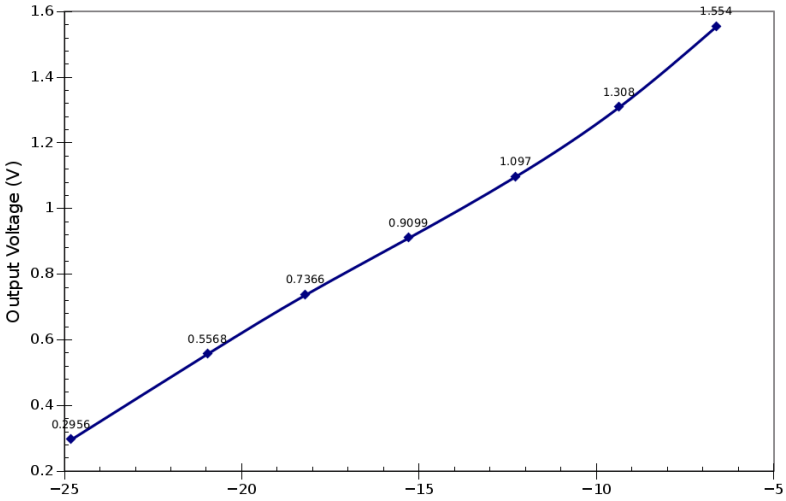


Figure 1.6: Output voltage as a function of input RF power in dBm.

As we can see in figure 1.6, the output voltage of the rectifier is an almost linear function of the input power in dBm. The output voltage is around 0.6 V at -20dBm input RF power, then doubles to around 1.2 V at -10dBm. Thus, ten times increase in the input RF power only allows twice the output voltage. Of course, we need to remember that the output power level of the rectifier is proportional to the square of the output voltage,

$$P_{out} = \frac{V_{out}^2}{R_L}$$

Nevertheless, it is clear that the power conversion efficiency of the inverter drops significantly then the input RF power rises from -20 dBm to -10 dBm. We could see this in the **power conversion efficiency** plot of the rectifier as shown in the following plot:

We could see that the PCE is sligthly below 0.8 at -20 dBm and slightly higher than 0.3 at -10 dBm, i.e. PCE drops by 2.5 times between these two power levels.

The reduction in PCE as the input RF power level increases is not totally disadvant-

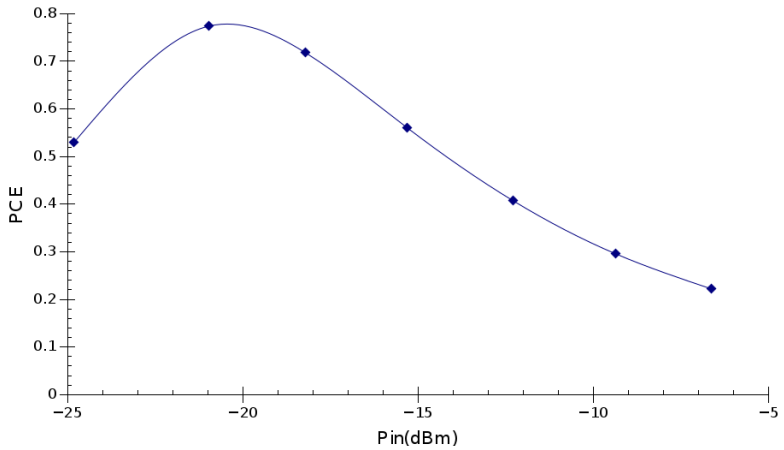


Figure 1.7: Power conversion efficiency of rectifier versus the input RF power in dBm.

ageous. Although it is out of scope here to go in to the details, the input power levels of an RFID tag can change between 6 dBm and -20 dBm, i.e. 400 times [**DanielM.Dobkin234**]. Even accounting for the quadratic relationship between the output voltage and power, the output voltage could increase by around thirteen times if the PCE were to be constant. If the output voltage at -20 dBm input RF power level is 0.6V, at 5 dBm the output voltage would increase to more than 7.8 V exceeding the the supply voltage limits of a typical 180nm CMOS process by around at least 5 V. The reduction in PCE to less than 0.2 at high input power levels means that the output voltage would stay much lower if PCE were to stay constant.

The next question we need to answer is whether this design is usable for a passive UHF RFID transponder chip. In a typical passive RFID transponder chip, the most of circuits would be operating at the subthreshold region of operation. Nevertheless there are limits to how much the supply voltage could be reduced. The lower supply voltages imply that the f_t of the MOSFETs are also reduced limiting the highest operating frequency of the various circuits, e.g. the ring oscillator.

Without going in to further details, we will assume that the chip would need two different supply levels when being read by and being written by an RFID reader as shown in table 1.4:

If we refer to the output voltage vs. input RF power level plot in figure 1.6, the reader could see that reading from and writing to the RFID tag could be only possible when

Read		Write	
min	max	min	max
1 V	2 V	1.6 V	2 V

Table 1.4: The required supply voltage ranges during read and write operations.

the input RF power is at least around -12 dBm and more than -5 dBm, respectively. This simulation does not include any parasitics due to interconnects and other circuits that are connected to RFID input port, such as the modulator and demodulator circuits. Therefore, we need to allow at least another 3dB loss in the rectifier input power to account for these effects, reducing the input sensitivity to -9 dBm during read operation.

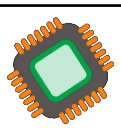
On the other hand, the best UHF RFID transponder chips in the market claim -18 dBm sensitivity. As we have seen from the earlier discussion, our differential-drive CMOS rectifier's output voltage at this power level is less than 0.7 V even without accounting for the losses due to the layout parasitics. How is that possible?

The answer lies with the fact that we could connect more than one rectifier in series to increase the output voltage even further. The design of such multi-stage RF-DC rectifiers and the inevitable compromises in the design process will be the subject of the next section.

DESIGN OF MULTI-STAGE RF-DC RECTIFIERS

In the last section, we concluded that a single stage rectifier cannot account for the minimum operational power of the present generation of the passive UHF RFID transponder integrated circuits (see page 12). To increase the rectifier output voltage further, we need to cascade more than one stage of the rectifier stages. Figure 1.8 shows a two-stages rectifier circuit. Both stages are assumed to be identical in the rest of the discussion here, although they do not ought to be.

Interstage capacitance C_{i1} is not strictly necessary but will be essential to stabilize the voltage at source of M2 and M4 PMOS transistors and filter out any high-



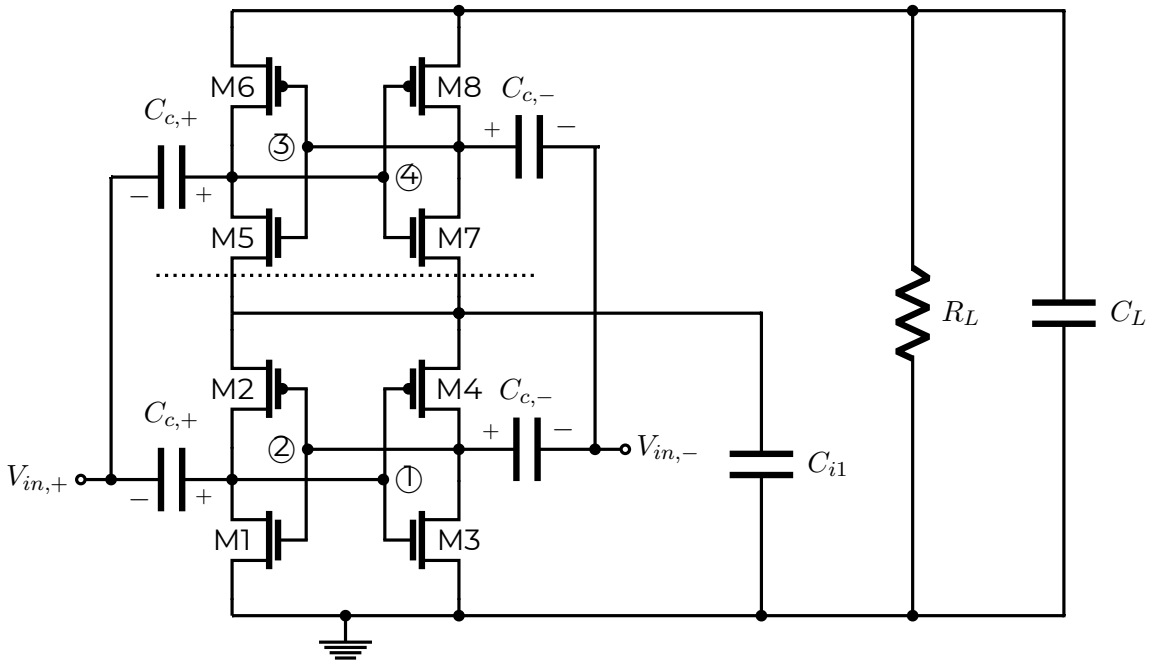


Figure 1.8: Differential Drive CMOS Rectifier Circuit

frequency disturbance at that node. The reason for this is due to the fact that the currents charged and discharged by the four inverters connected to that node will not completely cancel each other over a period of the input RF signal.

NMOS transistors M5 and M7 at the top rectifier stage would have higher threshold voltages than M1 and M3 at the bottom rectifier stage due to the body effect leading to decrease in power conversion efficiency for the top rectifier stage. If the CMOS fabrication process includes a deep n-well option, then the body-effect on the threshold voltage can be avoided by placing M5 and M7 in their own p-well inside a deep n-well and shorting the sources and the p-well taps can remove the body effect. On the other hand, the junction capacitance between the p-well for M5 and M7 and deep n-well, normally connected to the positive supply, will create a capacitive leakage path and reduce the power conversion efficiency.

Similarly, M2 and M4 can share a common n-well where their sources and substrate taps are shorted. The parasitic capacitance due to n-well/p-substrate junction will add to C_{i1}.

In figure 1.9, the power conversion efficiency vs. input RF power is plotted for recti-

fiers with one, two and three stages. We can observe two important behaviours in this plot:

1. The peak power conversion efficiency is slowly decreasing from around 78% to around 73% as the number of the cascaded stages in the rectifier keeps increasing due to inevitable losses of power transmission between the stages.
2. The peak power conversion efficiency happens at increasingly higher input RF power levels. For one stage rectifier, the peak PCE happens around at -20 dBm input RF power, while the peak PCE occurs at an input RF power level higher than -10 dBm.

   A corollary of this observation is that rectifiers with lower number of stages are more efficient at lower input RF power levels, while the rectifiers with higher number of stages are more efficient at higher input RF power levels.

   We should remember that we really would like to have PCE high at the lower input RF powers when the power is at a premium and would prefer PCE drop at the higher input RF powers to reduce the rate of the increase at the output rectified DC voltage value.

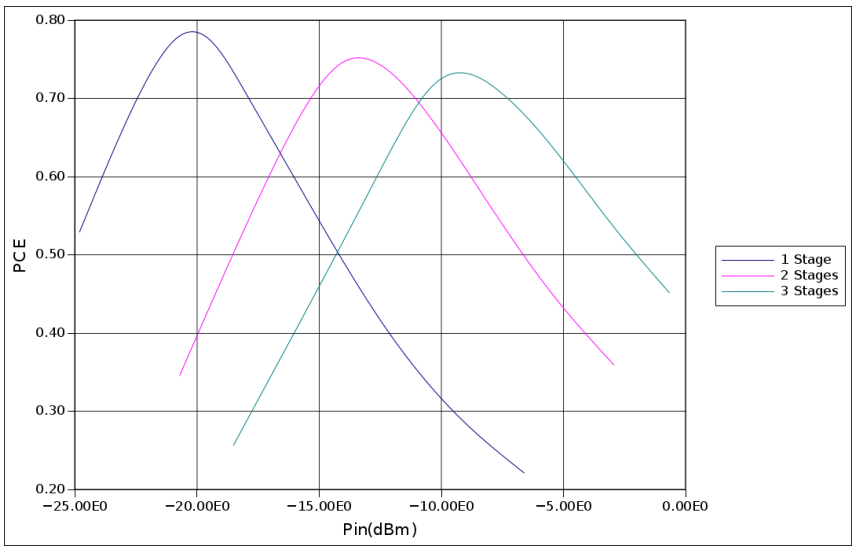


Figure 1.9: PCE versus the input RF power comparison for rectifiers with 1, 2 and 3 stages.

The next figure (figure 1.10) show the rectified output voltage vs. input RF power for rectifiers with one, two and three stages. Once again, we can make the observation

that one stage rectifier would have an higher output voltage at input RF power levels less than -17 dBm. Between -17 and -11 dBm, a two-stages rectifier would have the highest output voltage value, and then three cascaded stages rectifier would output the highest output voltage for RF input powers higher than -11 dBm.

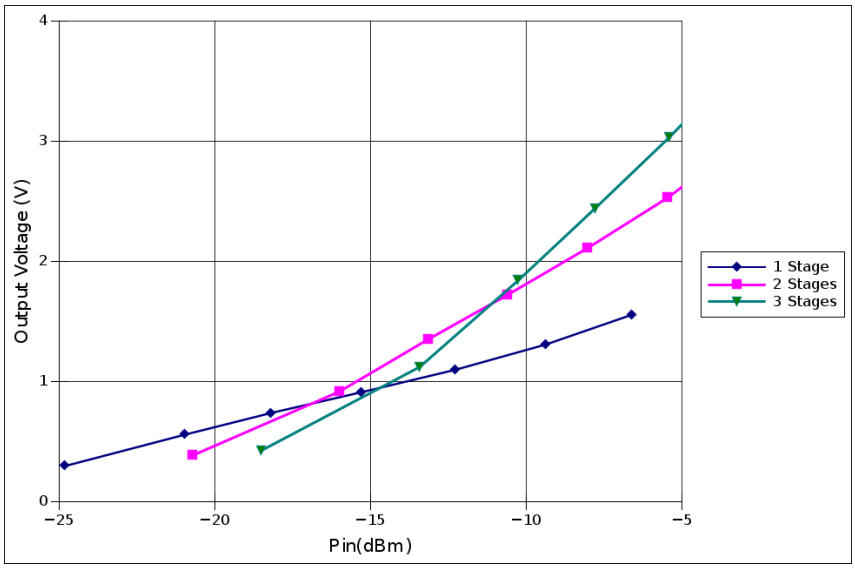


Figure 1.10: Rectifier output voltage versus the input RF power comparison for rectifiers with 1, 2 and 3 stages.

If we were to assume that the UHF RFID transponder chip requires at least 1 V rectifier output voltage (see table 1.4) when read from and 1.6 V rectifier output voltage when written to the tag, we could see that this particular rectifier design would need at least two stages. The minimum received RF power by the rectifier would need to be less than -16 dBm when read from and -12 dBm when written to the tag. Interestingly, adding another stage would not contribute the functionality of the transponder chip as the third stage really increases the output voltage over two stages design when the input RF power is higher than -11 dBm. When the input RF power level is at that level, we can also read and write the tag with a two stages rectifier. Another advantage of the 2-stages design over 3-stages rectifier design is that the former would have a lower output voltage at the high RF input power levels, easing the design of the DC limiter block.

SUMMARY

In this chapter, we reviewed the design of the fully-differential CMOS RF-DC rectifier design. We have shown that the ¨dynamic threshold compensation [3]¨ terminology for this type of circuits is a misnomer. Instead, the diodes in the basic diode-C rectifier circuit were replaced by MOSFET switches. Furthermore, we could view the resulting differential rectifier circuit as back-to-back connected CMOS inverters. Designing for the higher gains in these two inverters would decrease the time spent when both NMOS and PMOS devices are conducting and increase the power conversion efficiency.

We also reviewed the design of cascaded multi-stage rectifiers from a design perspective showing that 2-stages rectifier design was sufficient for the supply voltage specifications given in table 1.4. In fact, the increasing the number cascaded stages led to very high output voltages when the input RF power levels were high, i.e. when the tag was close to the reader.

Chapter 2

Rectifier Input Impedance Simulation and Measurement

INTRODUCTION

In the first part of this design note, the design of differential-drive CMOS RF-DC rectifiers were discussed starting from a simple diode-capacitor rectifier circuit. It was shown that the limitations posed by the relatively high turn-on threshold voltage of the silicon diodes could be overcome by replacing them by MOSFETs used as switches. Utilizing the differential nature of the RF signal output from the antenna, we could control the third terminal of these transistors, i.e. gates. Consequently, a fully-differential CMOS RF-DC rectifier circuit was designed. Finally, the behaviour of fully-differential rectifier over the input RF power was examined for behaviour of the output voltage value and rectifier's power conversion efficiency.

We have shown for a sample differential-drive CMOS rectifier that a single-stage rectifier stage's output voltage would not allow the RFID circuit to be read at the input RF power levels less than -12 dBm, if the minimum allowable supply voltage was assumed to be 0.9 V. We noted that this figure was around -6 dBm, i.e. 4 times, less than the best reported minimum RF power levels needed for UHF RFID tags to be successfully read.

This apparent contradiction was solved by using multi-stage rectifiers where more than one-stage of rectifiers are cascaded to reach to higher output voltages.

Another problem the designers face when designing UHF RFID transponder circuits is to understand the input impedance of the RFID chip to the antenna so that the tag antenna could be designed for the maximum power transfer from the antenna to the chip. We will not go into the details of the RFID tag antenna design, but will examine how the input impedance of the RFID chip can be simulated using a circuit simulator and measured using a VNA on the testbench.

INPUT IMPEDANCE

The input impedance of RFID chips are normally not designed to match a 50 Ω source impedance [6]. There has been some work regarding the matching of the input impedance of the RFID transponders to 50 Ω using on-chip passive elements, but they have not found application in the industrial settings [7].

The RFID transponder integrated circuit designers are frequently confronted with the problem of choosing the right impedance for the RF source element in their simulations. The lumped element models for antennas are generally one-ports ignoring the impedance transformation function of the antennas [8, 9, 10]. Viewed from the air-interface of the antenna, an antenna acts to match the intrinsic impedance of the free space, $120\pi\,\Omega$, to the input impedance of the receiver. In [1], the antenna model includes the radiation resistance of the antenna as the source impedance. Although this is a reasonable assumption, the designer cannot know the radiation resistance of the tag antenna when the tag chip is still being designed. In this work, the source impedance is chosen to be equal to the free space intrinsic impedance, $120\pi\,\Omega$ in test bench due to the lack of a better alternative and to stress the impedance conversion nature of the antenna. Thus, the combination of the matching circuit and the chip's input impedance should match the free space impedance of 376.73 when looking from the antenna, i.e. Z_{inlay} in figure 2.1. Similarly, the impedance of the combination of the free space impedance and tag antenna impedance should be the complex

conjugate of the chip's input impedance, i.e.

$$Z^*_{\text{tag}} = Z_{\text{chip}}$$

Figure 2.1 shows a possible matching circuit in the schematic assuming a single ended input including a series inductance, L_{series} and a shunt inductor, L_{shunt} . As the rectifier is a differential-input circuit, the simulation test bench circuit would normally include an ideal balun block at the input to convert the single-ended output of the source into a differential circuit [11]. The common-mode potential of the source can be set at 0 V as the differential input signals are commonly coupled to rectifier's core by MIMCAPs.

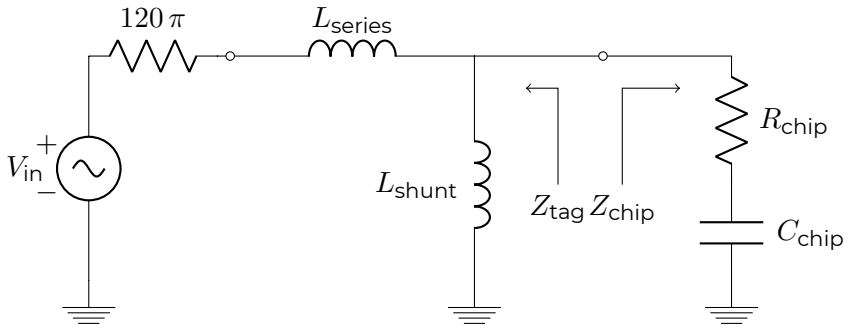


Figure 2.1: Lumped electrical model of antenna and chip input used in simulations.

A typical UHF RFID transponder chip would have R_{chip} between 15 and 25 and C_{chip} between 0.8 pF and 2 pF. The following table 2.1 summarizes the quoted values for the series input resistance and capacitance published by the chip manufacturers:

	EM Micro EM4124	NTLAB NT1025B	IMPINJ MONZA5	REVSEMI RVS101	Units
R_{chip}	25	16	27	19	Ω
C_{chip}	0.66	0.53	0.81	1.3	pF

Table 2.1: Series input resistance and capacitance values for some available UHF RFID chips.

In table 2.1, the input resistance values are quite close to each other, but the input capacitance values exhibit greater variation. It must be kept in mind that the measurement of the input impedance of an UHF RFID tag is not very precise. One reason

is the fact that the input impedance changes with the available input RF power level. The other reason that could affect the input capacitance values is how the de-embedding of the cables and connectors in the measurement setup is accomplished. We will look more closely into the measurement of the input impedance of RFID chips in the section 2.

INPUT IMPEDANCE SIMULATIONS

Analysis of the input impedance of the RF-DC rectifiers using the circuit simulators is complicated by the following facts:

1. The simulation of the rectifier would take a long time using transient analysis even when the load capacitance value is reduced to speed up the simulations for very small input power levels.
2. The relationship between the chip input port's voltage and input current is non-linear over a period of the input signal.
3. As mentioned above, the chip's input impedance will change with changing input RF power levels.
4. As the input current can be very small in order of nAs, the simulation tolerances should be tightened.

Here we will suggest a couple methodologies to overcome these difficulties. They represent our approach to this particular design problem, and we are sure that other approaches could be perfectly suitable. We will present our solutions in the order of the problems presented above:

SIMULATION TECHNIQUES

As alluded above, the transient simulations for the rectifier circuit would take a very long time to reach the steady-state when the input RF power levels are low. There a couple of reasons for this fact:

1. Low RF input power levels imply very low currents and voltages requiring tighter

absolute tolerances. Tighter simulation tolerances mean that the simulator needs to spend more time for the solving the circuit equations at each time-point.

2. For an input RF signal of 868 MHz, the period of the input signal is around 1.1 ns. Assuming that 50 µs is needed for the circuit to reach the steady-state [1], more than $50,000$ periods of the input signal ought to be simulated before the circuit reaches the steady-state condition. If at least 10 time-points for each period needed to accurately represent the behaviour of the currents and voltages, more than $500,000$ time points need be solved for before the circuit reaches the steady-state.

As seen from the discussion so far, the transient simulation of the rectifier circuits is time-consuming and discourages optimization of the circuit using PVT or Monte-Carlo type simulations where a large number of simulations have to be done.

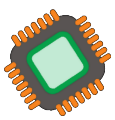
The solution is to choose the simulations involving shooting Newton type methods. They are known as *periodic steady-state analysis*, .PSS, in SPECTRE-RF and *Shooting Newton analysis* in HSPICE-RF simulators. By reusing the simulation state at the end of one simulation as the starting point for the next simulation and allowing for the necessary initialization time, a speed-up of the simulation durations up to 100 times can be reached.

As the input RF power levels increased, the circuit's behaviour will become more and more non-linear. Therefore a significant number of harmonics should be included in the simulation. A rule of thumb is to increase the number of harmonics until the circuit's behaviour does not change significantly in the simulations.

CALCULATION OF THE RF INPUT POWER AT THE RECTIFIER'S INPUT PORT

One of the frequent points of confusion in the design of RF rectifiers in an electronic design environment is how to define the input RF power to the rectifier. The customary S-parameter analysis in determining the input impedance of the chip is not

[1] ISO18000-6c standard allows up to 1.5 ms for the powering-up and initialization of the transponder.



meaningful as the the amplitude of the voltage signal at the input port of RFID chip could be more than 0.6 V when the input RF power is as low -15 dBm. Therefore we cannot easily determine a matching circuit between the RF port element and the circuit and add a limit on S11 parameter to ensure that most of the power from the RF port element is input the simulated circuit.

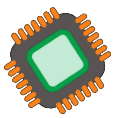
We need to approach the calculation of the input RF power to the RFID chip starting from the first principles. We need to recognize that what is important is how much total RF energy is absorbed by the chip over a period. Once the energy absorbed over one period is calculated, it is trivial to determine the average input power over that period.

To understand this point better, figure 2.2 shows the simulation results for the voltage across the input terminals, the input current, instantaneous input power and cumulative energy input over a period of the input RF signal. We assume that the input port of the transponder chip is directly connected to a source with an impedance of 376.3 ohm, i.e. the chip is connected to ”free-space” without an antenna. The source is assumed to be supplying -12 dBm to a matched load. As could be seen from the last row of the figure 2.2, the total input energy over one period at the steady-state condition is only 2.5 fJ. The average input power over one period is then 2.2 µW or -26.6 dBm.

Examining the plots further, we notice that the voltage across the input port and the current into the input port is almost out-of-phase. As a result, the , the plot for the instantaneous input power, $I_{\text{inp}} \cdot V_{\text{inp}}$, shows that the input power almost completely cancels itself over one period. This could be better understood by plotting the cumulative integral of the input power over one period, as shown in the fourth row, yielding a total of only 2.5 fJ energy contribution by the input over one period.

For this circuit, we could determine the magnitude of reflection coefficient using the formula for the relationship between the incident, reflected powers and the reflection coefficient.

$$P_{\text{refl}} = \left(1 - |\Gamma|^2\right) \cdot P_{\text{inc}} \tag{2.1}$$



where P_{inc}, P_{refl} and Γ are the incident, reflected RF power and the reflection coefficient of the input port, respectively. Substituting the values for incident and reflected powers in the equation 2.1, we could calculate the magnitude of the reflection coefficient to be

$$\Gamma = 0.98$$

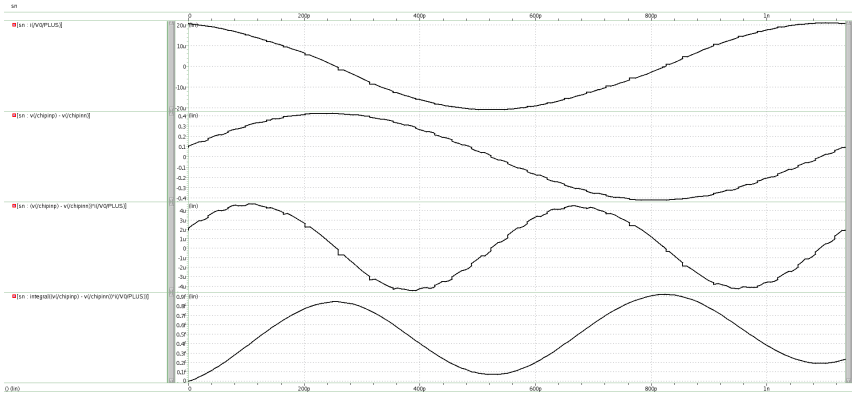


Figure 2.2: The input voltage, current, power and energy plots over one period.

A closer look at the input current waveform in the frequency domain would expose the non-linearities in the input impedance of the rectifier. Figure 2.3 shows the input current waveform when the source power to a matched load changes between -12 dBm and 6 dBm, corresponding to RF input power to the rectifier between -36dBm and -4dBm. The input current waveform exhibits increasingly larger contributions of higher odd-order harmonics. As the circuit is fully differential, the even-order harmonics comparatively suppressed.

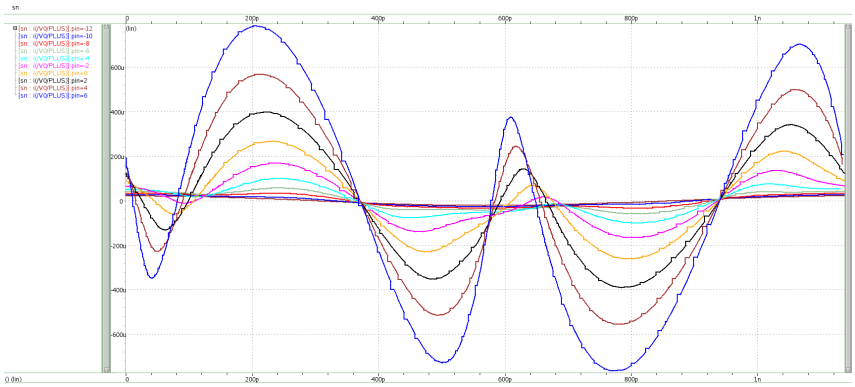


Figure 2.3: Input current of the rectifier when the source power is swept between -12 dBm and 6 dBm.

The next plot (figure 2.4) shows the results of shooting Newton AC simulations in HSPICE-RF showing the relative magnitudes of fundamental, third and fifth order harmonics of the input current. As could be seen from this plot, especially third order harmonic exhibits a very steep rise with the increasing input RF power, which explains the strongly nonlinear waveforms in figure 2.3.

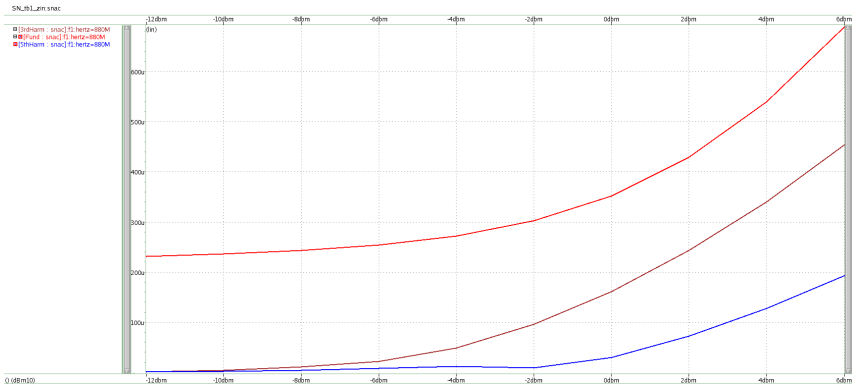


Figure 2.4: The plots of fundamental, third and fifth order harmonics of the input current.

ANALYSIS OF THE INPUT IMPEDANCE WITH SIMULATIONS

In summary, the input impedance is a non-linear function of the input RF power to the rectifier. This statement unfortunately does not help much the circuit designer charged with determining the input impedance of the rectifier or the whole transponder chip. There are some analyses presented in the literature for diode-based One possible methodology for determining the input impedance of the rectifier involves arriving at an estimate of the input resistance and capacitance by assuming that the input voltage and current are perfect sinusoids, a reasonable assumption at low input power levels. Once the input resistance and capacitance are determined, we could determine a matching circuit for the input impedance to the source impedance, in this case the impedance of free-space, 376.3 Ω.

A rudimentary proficiency of the Smith Charts would be useful in determining the matching circuit topology and the component values. Once the first-estimate for the component values are determined, either the optimization algorithms or simple parameter sweeps in the circuit simulator can be used to optimize the circuit such

that the all of the power transmitted by the source is absorbed by the rectifier. Please note that C_{chip} and R_{chip} in figure 2.1 model the rectifier's input resistance and capacitance at a certain input power level and would generally change with the changing input power values. We will further investigate this point when investigating the testbench measurement methodology for the input impedance of a UHF RFID transponder chip in section 2. An additional series capacitance, C_{series} would frequently be added in the matching circuit between the RF source and the inductors in figure 2.1 as the rectifier's input capacitance is much smaller than the total input capacitance of an RFID transponder chip.

In figure 2.5, the partial simulation results for a sample matching circuit optimisation run are shown. The series capacitance, C_{series}, is held at 0.3 pF, while the shunt and series inductances, L_{shunt}, and L_{series}, are swept between 0.1 µH - 0.2 µH and 0.4 µH - 0.6 µH, respectively. The source power to a matched load is -12 dBm. The optimum L_{shunt}, and L_{series} values are 0.13 µH and 0.5 µH, respectively, where the power absorbed by the rectifier indeed reaches -12 dBm, the value for a matched load to the source impedance. This observation also allows us to determine the input impedance of the rectifier circuit at a particular input power value.

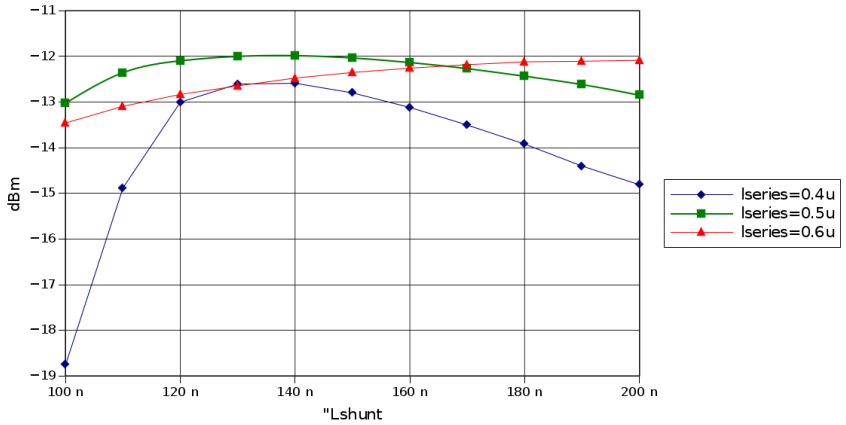


Figure 2.5: A sample series of simulation results for the matching circuit optimization for a rectifier.

If the power delivered by the source to a matched load is reduced to -15 dBm, the input impedance will be changed as well as evidenced by the following plot. The calculated input impedance for the rectifier circuit including TSMC's low-capacitance

ESD cells is $Z_{\text{in}} = (2720 - 1440\text{i})\,\Omega$.

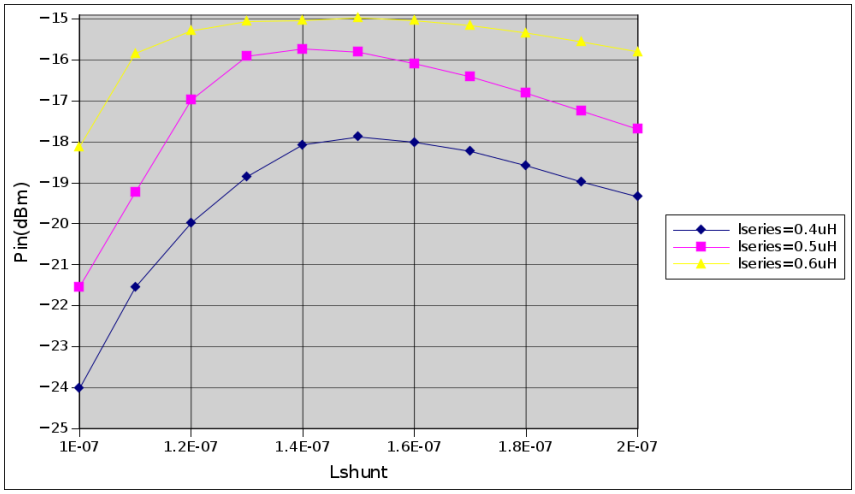


Figure 2.6: A sample series of simulation results for the matching circuit optimization for a rectifier when the source power level is reduced to -15 dBm.

In this section, we analysed the input impedance of an RF-DC rectifier starting from the first principles. As the rectifier circuit is constructed of strongly non-linear elements, i.e. MOSFETs, the relationship between the voltage across the input port and the input current is also non-linear. In fact, the rectifier would be reflecting some of the absorbed power during a portion of the input signal's period as evidenced by the plot in the third row of the figure 2.2.

INPUT IMPEDANCE MEASUREMENT

The measurement of the input impedance of passive UHF RFID chips has been covered in many articles in the literature[12, 13, 14]. The methodology first proposed by Kronberger et.al. [15] is preferred here as it is the simplest approach and yields the easily identifiable results for the input impedance.

The measurement of the input impedance of an RFID transponder chip presents unique difficulties:

1. The RFID chip is normally employed in flip-chip configuration, where the bare die is attached either to a strap which in turn is attached to the inlay or directly

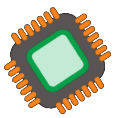
to the inlay. Therefore, the reference plane for the input impedance measurements should be carefully defined.

2. The reference plane should preferably be at the input pads of the flip-chip. To ensure that the measurement setup is calibrated, the calibration structures should be also included in the measurement setup.
3. As explained above in section 2, the input impedance of the transponder depends on the RF input power level.

When the input RF power to the rectifier is below the threshold power where the chip is activated and starts to draw current from the rectifier, the input impedance is more or less constant. When the input RF power reaches the threshold value, the rectifier begins to draw appreciable current from the source and input impedance drops. With increasing input RF power levels, the phase difference between input current and voltage begins to decrease causing an increase in the real part of the input impedance, i.e. input resistance.

The measurement setup is used in the bench tests is shown in figure 2.7. The board has two sets of the test fixtures including short, open, and load calibration configurations for both flip-chip and PLCC44 packaged chips. A National Instruments PXIe-5632 Vector Network Analyser was used to excite the chip and to measure the input impedance while the VNA's output RF power was swept between -10 to 10 dBm.

The next plot shows the measured series input resistance (cf. figure 2.1) values R_{in} for the RVS101 UHF RFID transponder chip. As could be seen in figure 2.8a, the chip is activated when the VNA output power level is around -1 dBm and the input resistance is equal to 19 Ω. The input capacitance at the threshold level of the RF input power could be calculated from the measured reactance value at 1 dBm VNA output power level, yielding a threshold power level of -10 dBm. This figure does not include the losses due to various connectors and cables between VNA output and chip input.



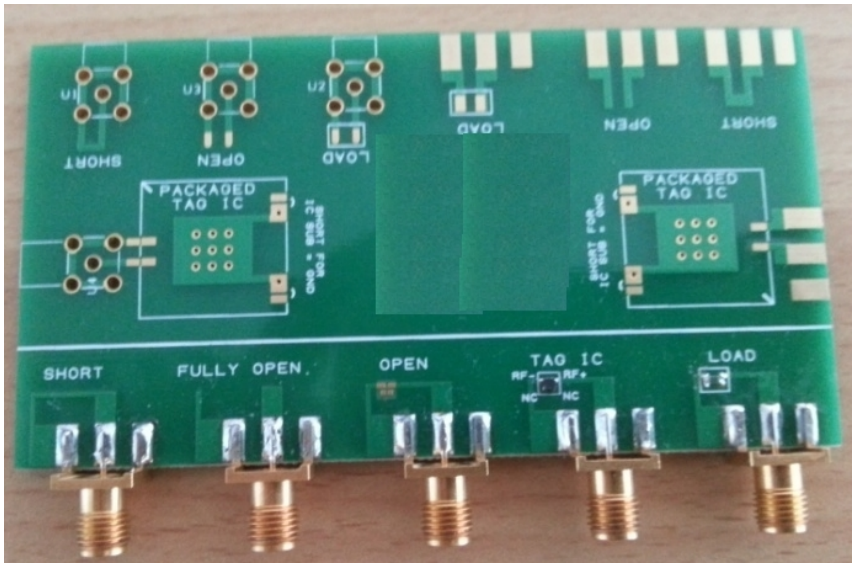
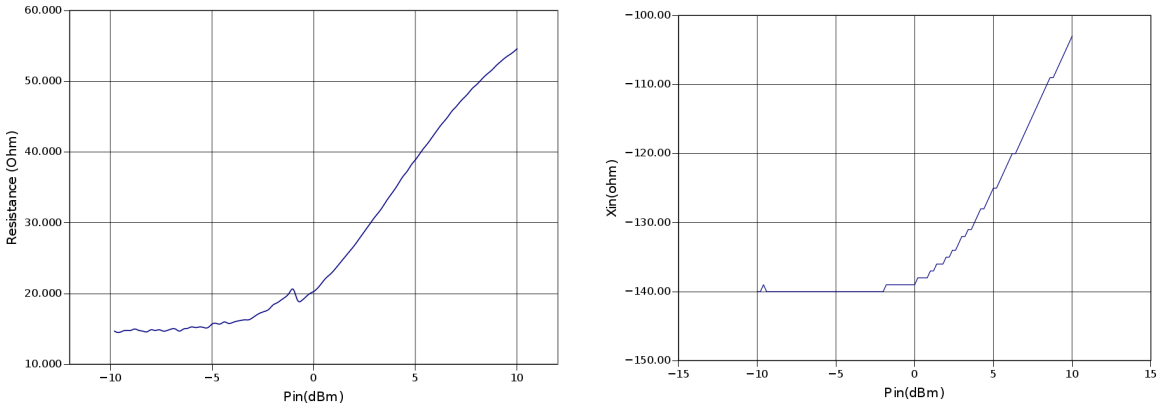


Figure 2.7: Revolution Semiconductor test board for the input impedance measurements.



(a) Input Resistance

(b) Input Reactance

Figure 2.8: Input resistance and reactance measurement results when the VNA output power is swept between -10 to 10 dBm.

SUMMARY

In this design note, we looked at the design of CMOS RF-DC rectifiers used in UHF RFID transponder chips. We have analysed one of the most promising topologies, differential-drive CMOS rectifier. The simulations for a sample single-stage rectifier was presented including the output voltage and power conversion efficiency figure of merit over a range of input RF power levels.

ACKNOWLEDGEMENTS

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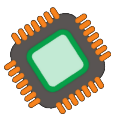

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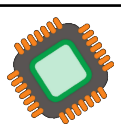

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